BOB DUNN

10/A/01

3366 COMPUTER LOGGER

MAINTENANCE HANDBOOK

THIS SPECIFICATION IS APPROVED
FOR USE IN THE CALIBRATION OF
COMPANY INSTRUMENTS.
5
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SERIES 3 COMPUTER LOGGER

The Modules and how they are operated.

The Series 3 Computer Logger consists of a Digital Equipment Corporation PDP-II computer, which is fitted with an interface to enable it to communicate with modules of the Compact 33 Data Logging System.

The Compact 33 modules become extensions of the PDP-II. They are operated by the computer and cannot communicate directly with one another, so that the data logging system can only be used under program control from the computer.

The addressing system of the PDP-II treats peripheral devices like computer memory locations, and a simple means of testing the functioning of a data-logging module is to address the module from the computer switch register by means of the "Load Address" key, and to examine its data on the computer lights by means of the "Examine" key, or to feed data to it from the computer switch register by means of the "Deposit" key.

Throughout this section the address and data lines will be numbered according to the PDP-II system, so that they correspond to the computer lights and switch register. Refer to the conversion table to convert these numbers to the numbering system used in the Compact 33 circuit diagrams. (Page 1.13).

Module Addressing

A module may be classified as a Source which supplies data to the computer, or a Receiver which accepts data from the computer. Each module has two addresses:

(a) Status/Control Address

This address can receive control information from the computer and supply status data to the computer.

(b) Data Address

This address allows data to be transferred to the computer for a Source, or to be received from the computer for a Receiver.

Most modules contain both Source and Receiver sections and consequently have four addresses.

Logger Highway Control

T_1	T_2	C233 Address BIT1
L	L	L
STATUS	READ	→ PROCESSOR (SOURCE)
H	H	H
DATA	WRITE	← PROCESSOR (RECEIVER)

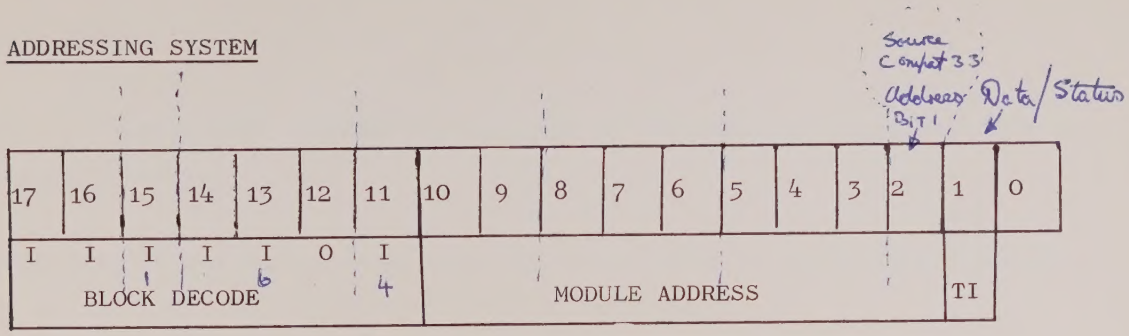
Typical Registers

64010	H	L	Rx	Status/control	} Command by processor to receiver or from processor eg set range + mode
64012	H	H	Rx	Data	
64014	L	L	source	Status	} Source of data for the processor e.g. D.V.M reading.
64016	L	H	source	Data	

CL33 address BIT1 (4 in computer address)

T1 (2 in computer address)

ADDRESSING SYSTEM



The PDP-II Unibus has an 18-bit addressing system. Bits 11-17 are de-coded in the interface and generate control signals. Bits 2-10 are fed to the logger address highway to be decoded by the logger modules. Bit 1 is converted into the logger Transfer 1 line (select status). Bit 0 (Byte selection) is not used in the logger system.

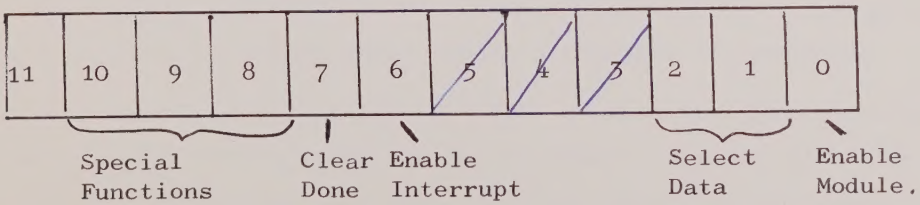
The Unibus control line C 1 is converted into the logger Transfer 2 line (~~select-source~~). The C 0 line is not used in the logger system.

Thus the logger modules are assigned a block of addresses from 164 000 to 167 776, of which the addresses from 166 000 to 167 776 are reserved for Compact 33 programmer modules.

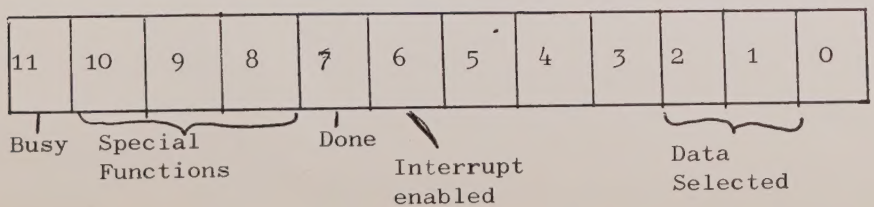
Each module issues an Address-Valid signal when it is addressed. If this signal does not appear within about 20 microseconds, then the processor forces a trap at vector location 004.

STATUS WORD BIT ASSIGNMENT

FROM the Computer Control Module is receiver



TO the Computer Status Module is source



DATA WORDS

Data is transferred between the low byte of the computer (Bits 0-7) and the logger modules.

According to the module concerned, the data may be in 8-bit binary format, or in two 4-bit BCD decades or in 8-bit ASCII code.

INTERRUPTS

Each Source or Receiver module has an individual interrupt-enable bit, which may be set or cleared under program control. When the module "Done" bit is set, if the "Interrupt-Enable" bit is also set then the module asserts the Interrupt-Search line on the logger highway.

When this line is asserted the interface carries out an Interrupt-Search routine, testing each status address in the logger until it finds an address at which the Interrupt-Enable bit and the Done bit are both set. The Vector Address of the module is then computed by adding 300 (octal) to bits 2-9 of the module address.

The interface will then make an interrupt request to the computer. The normal bus transfer sequence is put into operation within the computer to transfer bus master to the interface. The interface will pass the vector address to the computer and assert the INTR line, thereby initiating the normal interrupt action and entry into the service routine.

The interrupt search time is about $1\frac{1}{2}$ microseconds per module address (some addressed modules may not be present). The priority of a module is a function of its address.

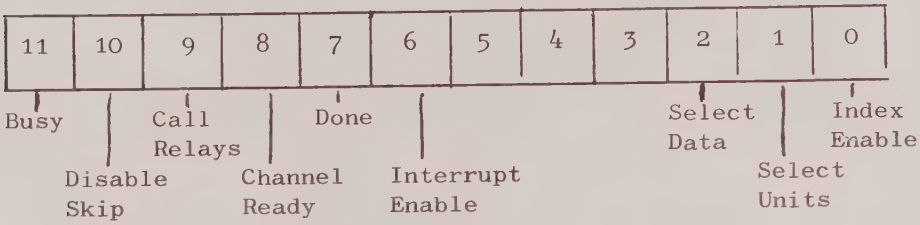
If the computer requests a data transfer during the interrupt search, the search routine is frozen until the data transfer is complete.

Module addresses are normally kept low so that the corresponding vector addresses avoid program locations in the memory. Typical addresses are quoted in the sections on the individual modules. These may not apply to all computer systems, and they do not apply to Compact 33 systems.

3353 SCANNER CONTROLLER

This drives the 3301 scanner system. It contains a Receiver section which receives channel setting information from the computer, and a Source section which supplies channel identity data to the computer.

Receiver Status Register 164000



Bit 0 - Index Enable (write only)

Bit 1 - When cleared the hundreds and tens decades or program data are selected. When set the units decade is selected (read/write).

Bit 2 - Selects program data from 3308 or 3309 (read/write). Contact 33 on Sg.

Bit 6 - Interrupt enable (read/write).

Bit 7 - Done (read only).

Bit 8 - Channel ready (read only).

Bit 9 - Call relays (read/write).

Bit 10 - Disable skip (read/write).

Bit 11 - Busy (read/~~write~~).

The counter is loaded from the "Front Panel" channel input by setting bits 1 and 2 in the Status Register, and then issuing a "set" command to the Source Data Register.
An Initialise pulse clears bits 0, 1, 2, 6, 9 and sets bits 7 and 10.

Channel Selection

When a channel is selected, if bit 9 is not set, the controller becomes "Busy" during the skip test period (about 10 microseconds) and then changes to "Done" if the channel is present. The scanner relays are disabled by calling the 800 and 400 drive lines simultaneously. When bit 9 is set, the controller becomes "Busy" during the relay settling period (about 10 milliseconds) and then changes to "Done" if the channel is present.

Operating the Skip Circuit

There are three modes of operation:

(a) Bit 10 set

Any channel may be selected, whether it is present or not.

(b) Bit 10 not set, bit 0 not set

If an attempt is made to select a channel which is not present, the controller remains "Busy" and the channel identity remains at the channel selected.

(c) Bit 10 not set, bit 0 set

Attempting to select a channel which is not present causes the channel counter to step on until a channel is found.

Receiver Data Register 164002

PDP-11 Bit	7	6	5	4	3	2	1	0
Status bit 1 = 0	800	400	200	100	80	40	20	10
Status bit 1 = 1	8	4	2	1				

This register allows the channel identity to be loaded in two bytes, in BCD code.
The action of loading data into this register causes status bit 1 to be complemented.
An attempt to read data from this register sets the channel identity to 000.

Source Status Register 164004

This address provides access to the same register as the Receiver Status Register, and the same bits may be set, cleared and examined.
The difference between the addresses is that if bit 0 is loaded at this address, the channel counter is incremented by one.

Source Data Register 164006

This allows the channel identity to be read by the computer. The control by status bit 1 and the data assignment are the same as in the Receiver Data Register.

If an attempt is made to load data into this register, the original channel identity is unchanged but status bit 1 is complemented.

If status bit 2 = 1 this register contains 8-bit binary data from a scanner program unit.

Bits.

L.A. 164000 SET C I
Deposit 1000
L.A. 164002
Dep. 100 & 10 3-0
L.A. 164002
Dep. units 7-4

L.A. 164004 READ C.I.
Dep. 000000
L.A 164006
EX. 100 & 10
L.A. 164006 complementary states Set 1
Dep. 164006
L.A. 164006
EX. units

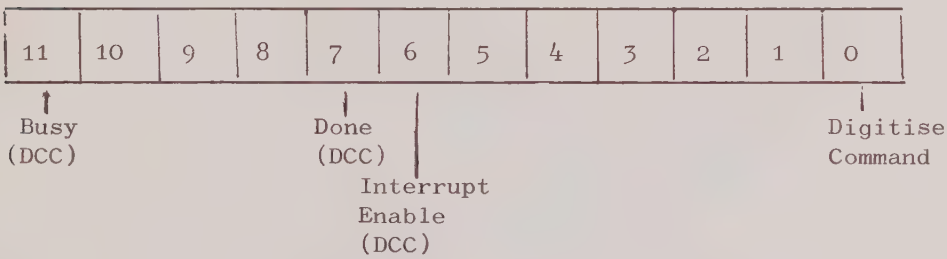
Master Voltmeter Interface 3336

This interface provides control signals and selects the data output from a Master Series Digital Voltmeter. It contains a Receiver section, which receives Range, Mode and Digitise Commands from the computer; and a Source section, which feeds the measurements from the digital voltmeter to the computer.

Master series voltmeters operate on a dual-ramp principle. The analogue input is sampled during the "Ramp-up" period, during which the "Data-can-change" signal goes to the "Busy" state. After the "Ramp-up" period, the "Data-can-change" signal returns to the "Done" condition, and the "Ramp-down" period occurs, during which the measurement is converted to a digital value. At the end of the "Ramp-down" period a "Print-command" signal is produced.

The two Status Registers of the interface allow independent use of the Data-can change and the Print-command signals. This allows the scanner to change to the next channel during the Ramp-down period, so that the maximum rate of scanning can be achieved.

Receiver Status Register 164010



Bit 0 - Digitise command (write only)

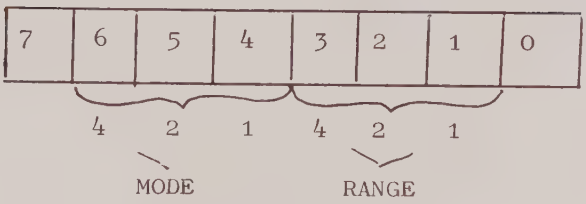
Bit 6 - Enables data-can-change interrupt (read/write)

Bit 7 - Data-can-change "Done" (read only)

Bit 11 - Data-can-change "Busy" (read only).

An Initialise pulse clears the register.

Receiver Data Register 164012



This register is write-only. Mode and Range information are fed to the digital voltmeter.

Range 0 - 1000 volt
" 1 - 100 "
" 2 - 10 "
" 3 - 1 "
" 4 - 100 millivolt
" 5 - 10 " ~~Errors on range 220~~ on A210 at 10 per sec goes to 1000V range only gets 10mV range at 25 ~~$100 per sec~~.

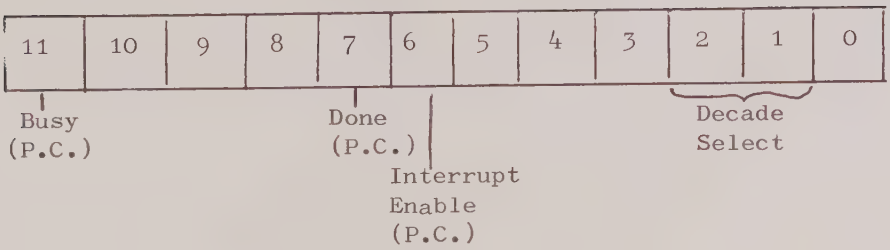
N.B. Range 5 is not available in some voltmeters of the Master series. Ranges 6 and 7 are interpreted as Range 0.

* Mode 0 - Local
* " 1 - Same as 3
" 2 - Remote 10/sec. Auto Range
" 3 - " 10/sec. Range as set
" 4 - " 25/sec. "
* " 5 - " 100/sec. "
" 6 - " AC "
" 7 - " OHMS "

N.B. All the Master series voltmeters contain the logic for commanding AC and OHMS, but the necessary analogue circuits are not fitted to all models. Modes 4 and 5 only apply to the A210 series.

* Errors on Basic

Source Status Register 164014



Bits 1 and 2 - determine which pair of decades are available from the Source Data Register (read/write)

Bit 6 - Enables Print-Command interrupt (read/write)

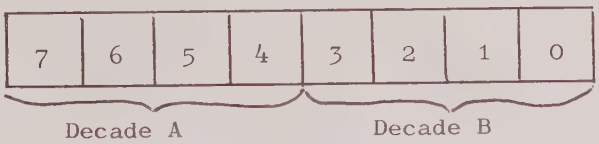
Bit 7 - Print-Command Done (read only)

Bit 11 - Print-Command Busy (read only).

An Initialise pulse clears the register.

Reading data from the Source Data Register clears the Print-Command Done bit.

Source Data Register 164016



This contains information from the digital voltmeter, in two decades, B.C.D. code.

If the voltmeter reading is + 0 1 2 3 4 5 R, where R is the range, the information may be read as follows:

Selection bits		Decade A	Decade B
2	1		
0	0	+	0
0	1	1	2
1	0	3	4
1	1	5	R

When fewer than six decades are in use, the information is truncated from the right, and spare decades contain zero. Polarity codes: + = 14

- = 13

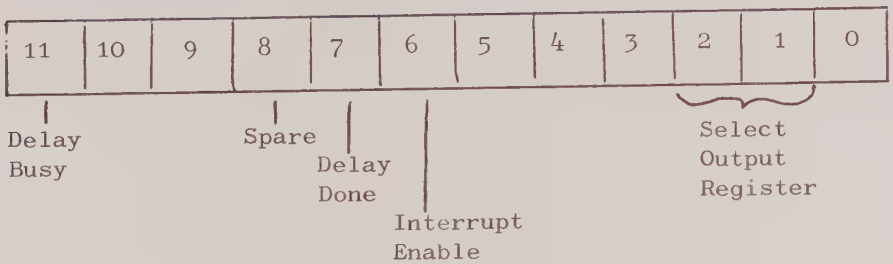
General Purpose Interface 3364

This contains 32 lamp/relay driver circuits and 8 input circuits. It also contains a timing circuit which may be linked to be triggered from various sources.

Receiver Status Register 164040

~~Source Status Register 164044~~

~~The status register is available at both addresses~~



Bit 7 - Normally set. Cleared during the delay period.

Bit 11 - Set at the beginning of the delay period.
Cleared from various sources according to link positions.

An Initialise pulse clears bits 1, 2, 6 and 11, and releases the lamp/relay drivers.

Receiver Data Register 164042

Bits 0 - 7 - Command eight lamp/relay driver circuits. Bits 1 and 2 of the Status Register determine which of the four groups of driver circuits is being commanded.

Source Data Register 164046

Bits 0 - 7 - Contain data from the eight digital input circuits.

Notes

N.B. > 5 VOLTS.

1) The input and output circuits can handle signals up to + 30 volts.

2) The delay timing components are not fitted until the particular requirements of the system are known.

3) The delay circuit may be triggered by one of the following signals, according to the position of links:

   (a) Reading data from the Source Data Register,

   (b) Loading data into the Receiver Data Register,

   (c) Loading data into the Receiver Data Register with the selection bits both set,

   (d) An external signal.

4) The same signals are also available for clearing the "Busy" bit if desired.

COMPACT 33 BUS CONNECTIONS

Pin No.	A (copper side)	B (component side)
1	ADDRESS bit 1	DATA bit 1
2	" " 2	" " 2
3	" " 3	" " 3
4	" " 4	" " 4
5	" " 5	" " 5
6	" " 6	" " 6
7	" " 7	" " 7
8	" " 8	" " 8
9	" " 9	INFORMATION bit 1
10	TRANSFER 1 (STATUS)	" " 2
11	TRANSFER 2 (READ)	" " 3
12	ADDRESS VALID	" " 4
13	STROBE	" " 5
14	MASTER RESET	" " 6
15	GROUP B **	" " 7
16	INTERRUPT SEARCH	" " 8
17	INTERRUPT 1 **	1 PULSE/SEC **
18	" 2 **	50 PULSES/SEC **
19	" 3 **	50 Hz **
20	" 4 **	+ 5 volts STAND-BY **
21	- 24 volts * (+ 48 volts * on Compact 33)	
22	+ 24 volts *	
23	+ 9 volts	
24	- 14 volts *	
25	+ 5 volts	
26	KEYWAY	
27	+ 5 volts	
28	COMMON RAIL	

* Unstabilised power supply. Measures about 30% high off load.

** not used in Computer-based Logger.

N.B. On all signal lines except interrupt lines 1-4, low is true.

CORRESPONDENCE BETWEEN PDP-11 UNIBUS AND COMPACT 33 BUS

PDP-11 Unibus	Compact 33 LOGGER UNIT.			
ADDRESS bit 1	TRANSFER 1 (STATUS) (Inverted)			
2	ADDRESS bit 1 L → PROCESSOR → H			
3	" " 2			
4	" " 3			
5	" " 4			
6	" " 5			
7	" " 6			
8	" " 7			
9	" " 8			
10	" " 9			
CONTROL LINE C1	TRANSFER 2 (READ) (Inverted)			
	STATUS		DATA	
	OUTPUT From PDP-11	INPUT To PDP-11	OUTPUT From PDP-11	INPUT To PDP-11
DATA bit 0	INFO bit 1		INFO bit 1	DATA bit 1
1	" " 2	DATA bit 2	" " 2	" " 2
2	" " 3	" " 3	" " 3	" " 3
3			" " 4	" " 4
4			" " 5	" " 5
5			" " 6	" " 6
6	" " 8	" " 8	" " 7	" " 7
7	" " 7	" " 7	" " 8	" " 8
8	" " 4	" " 4		
9	" " 5	" " 5		
10	" " 6	" " 6		
11		" " 1		

All signals are buffered in the 3363 interface.

All logic is LOW = TRUE.

3363 Interface

This is a printed circuit board which fits into one of the "Small Peripheral" positions in the PDP-11. It is connected by means of a 3387 cable to the 3360 Computer-Driven Controller in the Series 3 Logger Frame.

The Interface has the following functions:

(a) It generates control signals for data transfer between the PDP-11 Unibus and the Series 3 Logger.

(b) It contains buffer stages for the transmission of addresses and data.

(c) It performs a rearrangement of the data lines according to the conversion table, when a Status Register is being addressed.

(d) It contains Interrupt-control circuits to supply Vector Addresses to the processor and initiate Interrupt action.

Links are provided to select the Interrupt Priority level (normally set to level 4). 4 is the Lowest
7 " " Highest.

CONTROL INTERFACE 3360

The main function of the Control Interface 3360 is to identify any logging module that raises an 'interrupt' and to issue to the PDP11 Computer the interrupt request and 'vector' address relating to this module. The 3360 is located in the Computer Logger 3366 and operates in conjunction with the Computer Interface 3363, which is located in the PDP11 Computer. All data exchanges between the 3363 and the Computer Logger pass through the 3360.

The 3360 operates in two modes, one mode being concerned with programmed data transfers and the other with program interrupts.

Programmed data transfers have priority over the interrupts raised by the logging modules, by virtue of the ADDRESS AND MASTER SYNC. line. When this line is taken Lo by the 3363 it signifies to the 3360 that a programmed data transfer is called for by the Computer. If an interrupt identifying sequence is being performed by the 3360 when this occurs, then the sequence is halted until the programmed data transfer is completed; the interrupt identifying sequence then continues from the point where it was halted. During a programmed data transfer, control communications between the 3360 and the 3363 takes place on the TRANSFER and STROBE lines, and control communication between the 3360 and the logging modules takes place on the ADDRESS VALID and EXECUTE STROBE lines.

If no programmed data transfers are taking place, an 'interrupt search' is initiated by a logging module taking the INTERRUPT SEARCH line Lo. The sequence of events which follows is given in flow diagram form in fig. 1. On this diagram can be seen the various points at which the sequence is halted if a programmed data transfer is called. During an interrupt search, control lines T1 and T2 from the 3360 to the logging modules are both held Lo; thus, the status of the interrupting module, relating to 'INTERRUPT ENABLED' and 'DONE' is checked by the 3360, in addition to ADDRESS VALID. The 'vector' address which is issued by the 3360 at this time is obtained by multiplying the SEARCH ADDRESS COUNTER output by a factor of 4 and adding 300.

SCANNER CONTROLLER 3353

The Scanner Controller 3353 provides BCD channel selection data for 3300 Series Analogue Scanner modules, in accordance with information it receives from the system highways.

Address Decoder (DRG 3353930I SHT1)

The unique binary address of the Scanner Controller is set by links in the ADDRESS DECODE network; a link inserted corresponds to a Hi on the associated address highway line. On decoding its unique address, issued by System Controller, the ADDRESS DECODE network outputs a Lo 'address valid' signal to the system controller and also a Lo enabling signal to the COMMAND GATES network.

Command Gates (DRG 3353930I SHT1)

After receiving the 'address valid' signal from the Scanner Controller, the system controller outputs an execute strobe pulse which causes the COMMAND GATE network to function in accordance with the state of control lines T1, T2 and Address Bit '1'. The four main functions of the COMMAND GATES network are:-

i) to set the STATUS STORE in accordance with the status information applied to its inputs from the information highway.

ii) to gate the information contained in the STATUS STORE, through the STATUS GATES, onto the data highway.

iii) to load or 'index' the contents of the CHANNEL COUNTER in accordance with the information contained in the STATUS STORES.

iv) in accordance with the STATUS STORES information to gate either the contents of the CHANNEL COUNTER or the 'scanner program address' onto the data highway.

CHANNEL COUNTER (DRG 3353930ISHT2)

Under control of the COMMAND GATES the channel count can:-

i) be set to the BCD number put on the information highway by the system controller.

ii) be set to the BCD number present on the FRONT PANEL. F.P. CHANNEL LINK.

iii) be gated onto the data highway, through the DATA HIGHWAY GATES.

iv) be output to the front panel via the channel link.

Under control of the SKIP/INDEX LOOP the channel count can be 'indexed' i.e., incremented one channel at a time. An 'index' operation is initiated by a 'status' decode and is thereafter under direct control from the STATUS STORES.

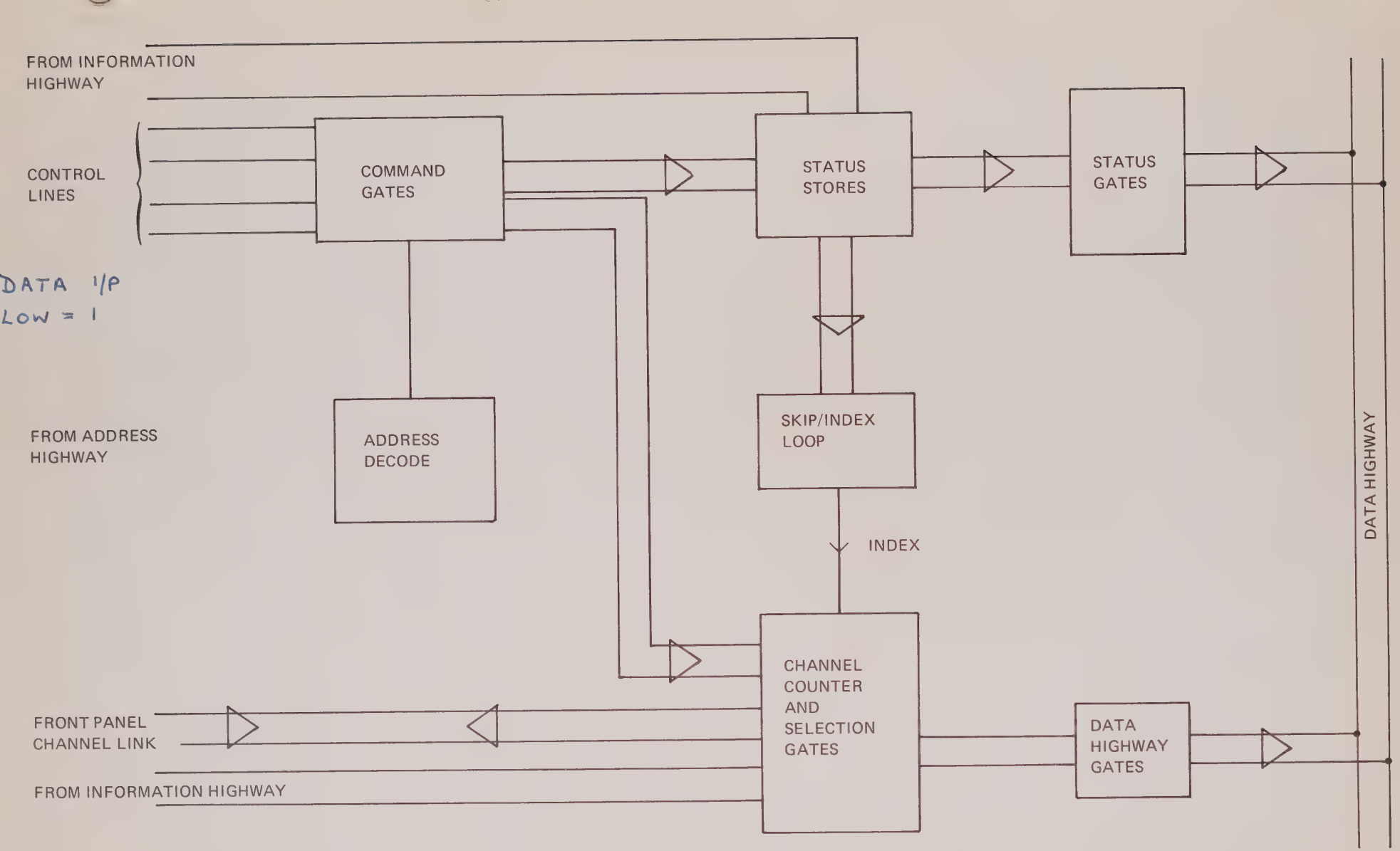
3353 (continued)

Channel Selection

When a channel is selected, a "Channel Ready" line, derived from the Selector Module, is tested after a 15-microsecond settling delay. If the channel is not present, the Scanner Controller may or may not step on until it finds a channel which is present according to the setting of the Status Store.

The relay on the selected channel may be switched on or off by the Status Store.

When the command is given to energise a relay, there is a delay of about 150 microseconds before the relay is energised, to produce a break before make action. After a further delay of 10-15 milliseconds, to allow the relay to settle, the Scanner Controller issues a "Done" signal to the Status Output Gates and also issues an Interrupt Search request on the System Highway, if its Interrupt is enabled.



SCANNER CONTROLLER 3353

3336 A200/A210 Voltmeter Interface

The 3336 DVM Interface provides remote selection of mode and range, and digitise commands for Digital Voltmeters of the A200 and A210 series, in accordance with information received from the system highways.

It supplies Status information from both stages of the voltmeter dual-ramp measuring cycle to permit the system to run at maximum speed.

It permits data to be fed in BCD code from the digital voltmeter to the system highways. It has provision for a polarity input (single-line control), six full decades for measurement data and one three-bit decade for range information.

Address Decoder

The binary address of the DVM Interface is set by links in the Address Decode network. A link corresponds to a high level on the associated address line (i.e. not called). When the system controller supplies the address of the module, the Address Decoder issues a low Address Valid signal to the system controller.

Control Gates

The Control Gates decode the system control lines T1, T2, Strobe and Address bit 1 to carry out the following control functions:

(a) To set the Status Stores in accordance with status information supplied to its inputs from the Information Highway.
(b) To gate the information from the Status Stores through the Status Gates to the Data Highway.
(c) To set Mode and Range information into the Function Stores from the Information Highway.
(d) To operate the Digitise Command circuit when commanded on the Information Highway.
(e) To set the Decade Selector in accordance with information from the Information Highway.
(f) To issue two decades of data to the Data Highway in accordance with the setting of the Data Selector.

Digitise Command Circuit

This circuit issues a Digitise Command pulse to the DVM Fan-out unit after a delay of about 7 milliseconds.
If the Mode information has been changed, this delay period is extended by about 75 milliseconds to allow the DVM circuits to settle.

Change of Data Circuit

If the Mode or the Range is changed, this circuit supplies a Data Has Changed signal to the DVM Fan-out unit.

Decade Selection

Selector bits		Output	
0	0	Polarity	Decade 1 (most significant)
0	1	Decade 2	Decade 3
1	0	Decade 4	Decade 5
1	1	Decade 6 (least significant)	Range

Links

The D links vary the mode of operation of the Decade Selector circuit.
In the computer-based logger, the selection bits from the information highway are stored in the Decade Selector Store before being used to select the decades for gating to the Data Highway.
In the Compact 33, the selection bits are fed directly from the information highway to the decade gates.

The S links select two-bit status words to be fed to the data highway in each of the four decade selection states. They are normally set to the same bit pattern as the command input, but alternatively the links may be used to provide information about un-used decades.

3364 DIGITAL INPUT/OUTPUT INTERFACE

The 3364 Digital Input/Output Interface, in accordance with information it receives from the system controller, performs two main functions:

i) it staticises data received from the information highway and uses this data to call up various external devices, such as relays and indicator lamps (receiver mode).

ii) it controls the flow of data from external devices, such as switches, onto the data highway (transmitter mode).

ADDRESS DECODE

FOR USE WITH BASAC CUTOUT LINK 4.

The unique binary address of the Digital Input/Output Interface is set by links in the ADDRESS VALID DETECTOR; a link inserted corresponds to a Hi on the associated address highway line. On decoding the unique address, the ADDRESS VALID DETECTOR outputs a Lo 'enabling' signal to the STATUS GATES and a Lo 'address valid' signal to the system controller.

SET STATUS

Register selection and 'interrupt' information that appears on the information highway is strobed into the STATUS CONTROL STORE by a Lo 'set status' pulse from the STATUS GATES.

READ STATUS

A Lo 'read status' level from the STATUS GATES opens the READ STATUS GATES and the DATA HIGHWAY GATES, thus allowing the state of the STATUS CONTROL STORE and the 'busy' and 'done' outputs of the INTERRUPT GATES to appear on the data highway.

DATA RECEIVE MODE

A Lo 'receive data' pulse from the STATUS GATES is applied, together with the register selection outputs of the STATUS CONTROL STORE, to the CONTROL DECODER network; the Lo pulse resulting from the CONTROL DECODER causes the data then present on the information highway to be stored in the appropriate register of the OUTPUT LATCHES.

DATA TRANSMIT MODE

A Lo 'transmit data' pulse, or level (depending on the position of LINK 'E') from the STATUS GATES opens the INPUT DATA GATES and the DATA HIGHWAY GATES, thus allowing the 'external' data to appear on the data highway.

INTERRUPT

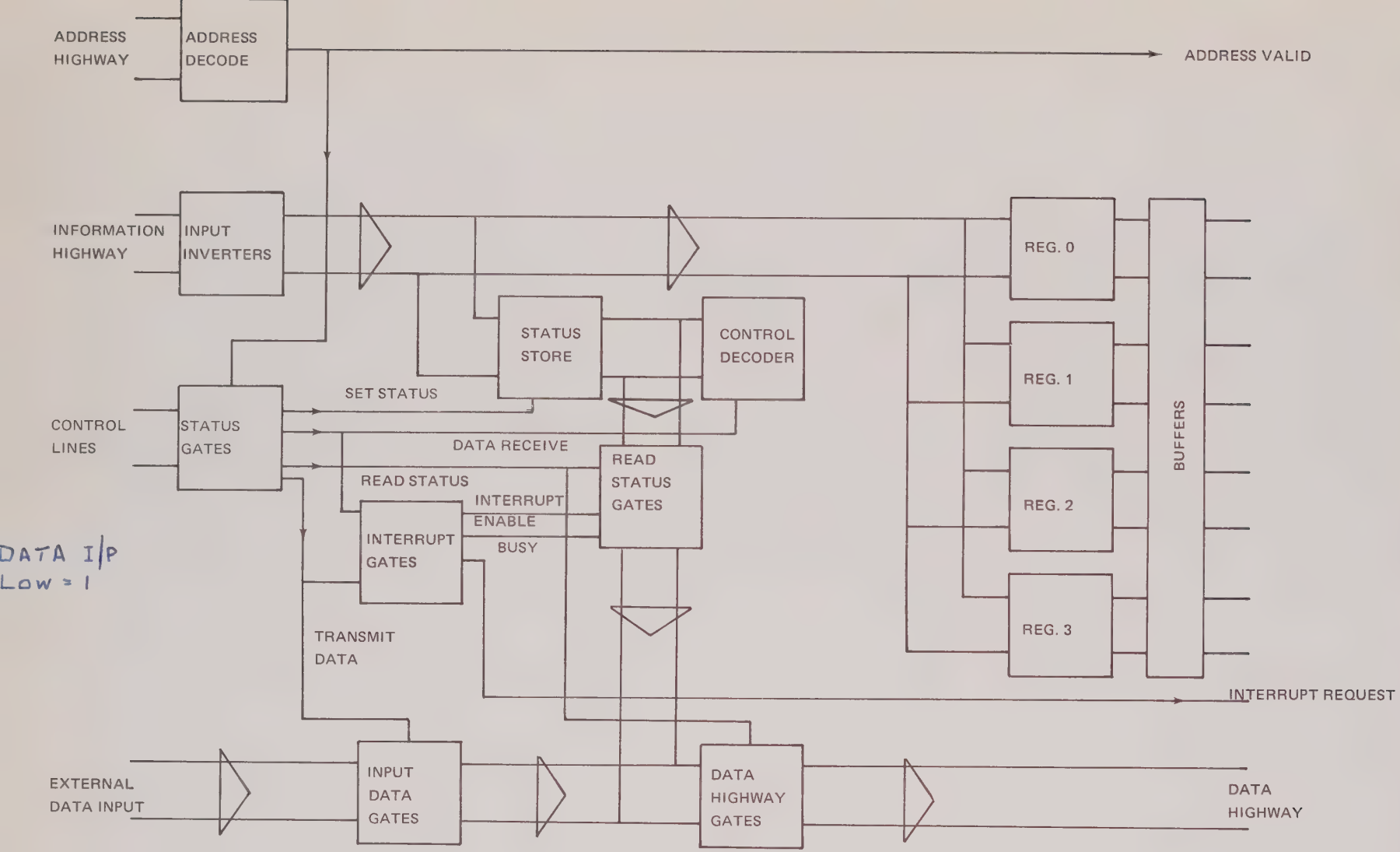
When the 'interrupt enable' latch in the STATUS CONTROL STORE is set, the INTERRUPT GATES take the 'interrupt search' line Lo on completion of a 'receive data' or a 'transmit data' operation. A 'busy' output from the INTERRUPT GATES (IC17, $\bar{Q}$) is taken Lo for the duration of each step in a 'receive data' or 'transmit data' operation, regardless of the state of the 'interrupt enable' latch.

3364 Digital Interface

Connections to PLB

[redacted]	1a	COMMON OF SUPPLY (+24V)	
Common Rail	1b		

Output Connections		Input Connections	
Register 0 bit 1	2a	Bit 1	19a
" " 2	2b	" 2	20a
" " 3	3b	" 3	19b
" " 4	3a	" 4	20b
" " 5	4a	" 5	21a
" " 6	4b	" 6	22a
" " 7	5b	" 7	21b
" " 8	5a	" 8	22b
Register 1 bit 1	6a		
" " 2	6b	External Interrupt	18a
" " 3	7b		
" " 4	7a		
" " 5	8a		
" " 6	8b		
" " 7	9b		
" " 8	9a		
Register 2 bit 1	10a		
" " 2	10b		
" " 3	11b		
" " 4	11a		
" " 5	12a		
" " 6	12b		
" " 7	13b		
" " 8	13a		
Register 3 bit 1	14a		
" " 2	14b		
" " 3	15b		
" " 4	15a		
" " 5	16a		
" " 6	16b		
" " 7	17b		
" " 8	17a		



DIGITAL INPUT/OUTPUT INTERFACE 3364

3333 POWER UNIT

1. ENVIRONMENTAL REQUIREMENTS

1.1 Temperature

Operating: $0^{o}C$ to $+50^{o}C$. Storage: $-10^{o}C$ to $+85^{o}C$.

1.2 Humidity

80% RH maximum.

1.3 Mechanical

To meet Solartron Specification 50/01/102.

2. ELECTRICAL REQUIREMENTS

2.1 Input

2.1.1 Supply: Design values: 117V or 234V + 10% - 15% 48-65 Hz. To be selected by a MAINS INPUT SELECTOR mounted on the Panel which will be marked 115V and 230V. When operated on the appropriate tape the Unit shall meet the specifications for outputs over the full range of supply input.

2.1.2 Switching: Mains ON/OFF will be a switch not mounted on the Power Unit. The Power Unit will incorporate the LINE and NEUTRAL connections to and from this switch.

2.1.3 Fuses: The mains input shall be fused in the LINE conductor before the filter (4.1.4)

Fuse ratings: Input 115V 13A HRC Beswick TDC 180
Input 230V 7A HRC Beswick TDC 180

There shall be a second fuse in the LINE conductor after the ON/OFF switch in the input to this Power Unit.

Ratings: 115V 6.3A Slo Beswick S503
230V 3.15A Slo Beswick S503

2.1.4 Filter: A mains input filter shall be incorporated between the first fuse and the ON/OFF switch. Circuit and values are shown in Fig. 1. (See also 4.10 AC Outputs)

2.1.5 Connector: Mains input, mounted on Panel, is to be: either SWITCHCRAFT EAC 301 - Agent: Sourian Lectropon or PERENA 3315-31-01-01 - Agent: Guest International.

2.2 D.C. Output 1

2.2.1 Output 1 Nominal +5V at 12A maximum. Adjustable from 4.8V to 5.2V with a resolution not worse than 50mV. Remote sensing is to be provided and the specified parameters are to apply at the point of remote sensing.

2.2.2 Stabilisation: Better than 0.1% over supply variation in Section 4.1.

2.2.3 Regulation: Better than 0.1% for load change of 5A to 12A.

2.2.4 Impedance: <10mΩ dc to 10kHz. <100mΩ 10kHz to 100kHz.

2.2.5 Ripple: (inclusive of all spikes and pick-up) <5mV peak to peak.

2.2.6 Temperature Coefficient: <0.02%°C.

2.2.7 Transient Recovery: For a step change of 5A to 10A load, output will be within 50mV of final value in <20μs.

2.2.8 Overvoltage Protection: If the output voltage exceeds the trip level a protection circuit must rapidly reduce the voltage to a safe value. Trip level to be supplied set to 5.75V ±0.1V. Using the test circuit of Fig. 2. the voltage is to reduce to 6V in <20μs from firing the thyristor.

2.2.9. Overcurrent Protection: At a load >12A but <15.5A the output voltage of both Outputs 1 and 2 are to fall to near zero. This trip is to automatically reset after 0.5s to 2.0s.

2.2.10 Fuse: 13A HRC (Beswick TDC 180)

2.3 D.C. Output 2

2.3.1 Output 2: Nominal +9V at zero to 2A.

2.3.2 Variation: Total excursion not to exceed ±0.4V at any combination of operating conditions within this specification.

2.3.3 Temperature Coefficient: <0.05%°C.

2.3.4 Ripple: (including all spikes and pick-up) <50mV peak to peak.

2.3.5 Overcurrent Protection: At a load >2A but <2.7A the output voltages of both Outputs 1 and 2 are to reduce to near zero. The trip is to reset after between 0.5s and 2.0s.

2.3.6 Fuse: 2.5A HRC (Beswick TDC 14).

2.4 D.C. Output 3

2.4.1 Output 3: -16.0V ±0.5V at 1.25A maximum unregulated. The nominal voltage to be obtained at nominal mains and 1.25A load.

2.4.2 Regulation: Output change of <3V for load change zero to 1.25A.

2.4.3 Ripple: <2V peak to peak at 1.25A load.

2.4.4 Fuse: 1.6A HRC (Beswick TDC 14).

2.5 D.C. Output 4

2.5.1 Output 4: Either 12V ± 0.5V at 1A maximum)
Or 24V ± 1V at 1A maximum) either positive or negative
Unregulated at nominal mains input. Voltage and polarity to be set by internal soldered links. TO BE SUPPLIED LINKED FOR +24V.

2.5.2 Smoothing: At least 3000µF.

2.5.3 Fuse: 1.6A HRC (Beswick TDC 14).

2.6 D.C. Output 5

As for Output 4. TO BE SUPPLIED LINKED FOR +24V.

NOTE: Outputs 4 and 5, alternative to separate use, must be able to be combined in parallel or in series, by internal soldered links, to give any one of the following:

±12V at 2A)
+24V at 2A) At either Output 4 or 5.
−

+ 36V at 1A)
+ 48V at 1A) At output

- 36V at 1A)
- 48V at 1A) At output

2.7 Square Wave Output

2.7.1 Output 6: Square wave 5V peak to peak at mains frequency:
At OV : output resistance not less than 100Ω.
At +5V : output resistance not greater than 1kΩ.
OV = 0 to +0.4V.
5V = 3.5 to 5.25V.

2.8 Common Rail

Outputs 1 - 6 are referred to one common OV.

2.9 A.C. Outputs

The mains supply, filtered but NOT switched, shall be available at 4 outlets, BULGIN SA2026, on the Panel. Total capacity 4A at 230V.

HIGH SPEED PUNCH/READER INTERFACE 3369

The 3369 is located in the PDP 11 Computer. It controls the transference of data from the H.S. Reader to the Computer and from the Computer to the H.S. Punch.

INSTALLATION INSTRUCTIONS

M105 Address Selector Module PERIPHERALS ~~HANDBOOK~~ H/BOOK P. 6-9

Remove all address links except 4 and 7.

M7820 Interrupt Control Module PERIPHERALS H/BOOK P. 6-26

Remove vector - address links 3, 4 and 5, leaving links 6, 7 and 8 in position.

The interface fits into one of the "Small Peripheral" positions in the PDP 11. Remove the G727 Grant Continuity link card from position D, and fit the modules as shown in the diagram (any vacant row may be used).

	A	B	C	D	E	F
1				G727		
2				G727		
BACK 3			3369 Interface		M105	M7820
4				G727		

DD 11-A Mounting Assembly MODULE SIDE

CAUTION

The High Speed Reader and/or H.S. Punch logic is isolated from mains earth, and decoupling capacitors which are fitted may develop a high voltage charge if the power is applied to the unit when it is not connected to the interface. To avoid damage, caused by discharging these capacitors through signal paths, ENSURE THAT THE MAINS LEADS OF THE UNITS ARE ISOLATED FROM THE SUPPLY BEFORE CONNECTING THE SIGNAL CABLES TO THE INTERFACE.

LINKS

Links are provided to change the phase of the reader data, punch data, reader step, punch feed, reader ready and punch ready signals.
By linking 59 - 60 (A) the reader circuit can run without a ready signal.
By linking 55 - 56 (D) the punch circuit can run without a ready signal.
By removing the link 63 - 64 (B) the reader can be driven by a short step pulse instead of a level.

Links are provided to change the Bus Request and Bus Grant priority level (normally set to level 4).

THEORY OF OPERATION - 3369

PUNCH

The Status Register (normal address 177554) is selected by the Select 4 line.

Bit 6 = Interrupt enable (read/write)
Bit 7 = Punch done (read only)

An Initialise pulse clears bit 6 and sets bit 7. Via IC18, PIN14 + IC13 PIN2.

The Data Register (normal address 177556) is selected by the Select 6 line.

When a character is loaded into this register it causes the punch to punch that particular character.

The interrupt-enable bit, bit 6 (Bus 06), is fed via IC8 pin 2 to IC24 pin 2.

IC24 is clocked by the Select 4 Signal on IC22 pin 13.

When a character is loaded, the pulse from IC22 pin 10 clocks the data registers IC5 and 6, and fires Mono IC16, which provides a punch-feed pulse and clears the done flip-flop IC24b.

When the punch has completed the character, the punch-ready input fires Mono IC26 which clocks IC24b to the Done condition.

READER

The Status Register (normal address 177550) is selected by the Select 0 line.

Bit 0 = Reader step (write only)
Bit 6 = Interrupt enable (read/write)
Bit 7 = Reader done)
Bit 11 = Reader busy) (read only)
Bit 15 = Reader error)

An Initialise pulse clears the status register.

The data register (normal address 177552) contains the character from the reader. The reader-done bit (bit 7 of status register) is cleared when the data register is read by the program.

A reader-step command, consisting of bit 0 via IC8 pin 13, from IC12 pin 11 fires mono IC20, which sets the Busy flip-flop IC10b, and clears the Done flip-flop IC15b. The Busy flip-flop produces a reader-step output which drives the tape reader. When the next feed hole is detected, the feed-hole signal (reader ready) fires mono IC11, which clocks the Busy flip-flop, which then clocks the Done flip-flop.

The reader-step pulse from IC20 also fires the re-triggerable mono IC19 (10 mS). If the pulse from IC19 terminates while the Busy flip-flop is still set, the output from IC23 pin 8 provides an error signal, and also a reader interrupt if the interrupt is enabled.

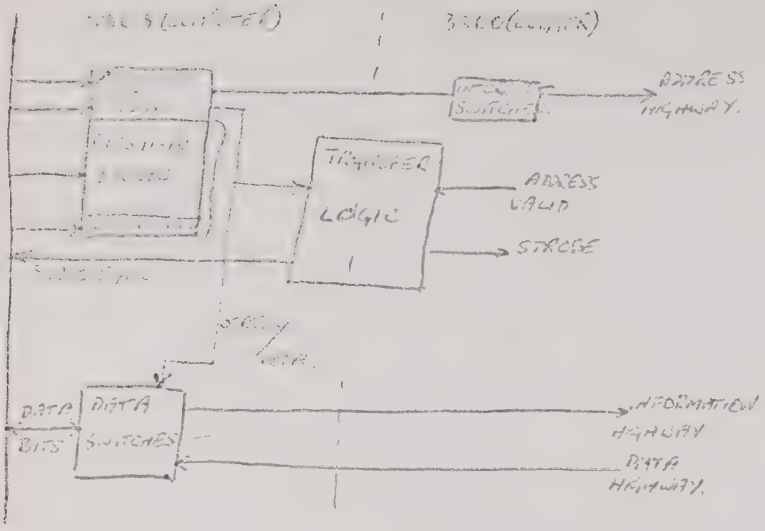
PUNCH CONNECTIONS PL1

Pin	Function
B1	Bit 4
B2	" 3
B3	" 7 (Most significant)
B4	" 6
B5	" 0 (Least significant)
B6	" 2
B7	" 5
B8	" 1
B9	COMMON RAIL
B10	PUNCH FEED
B11	PUNCH READY
B15	KEYWAY

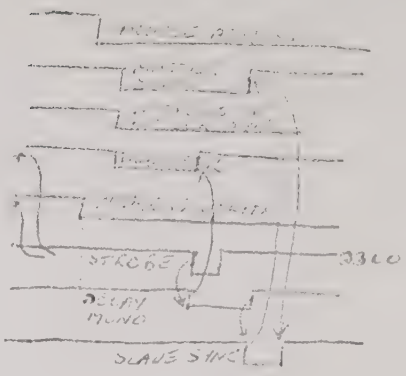
READER CONNECTIONS PL2

Pin	Function
B1	Bit 7 (Most significant)
B2	" 4
B3	" 5
B4	" 2
B5	" 6
B6	" 0 (Least significant)
B7	" 1
B8	" 3
B9	READER STEP (- 12 volt)
B10	EXTERNAL - 12 volt SUPPLY
B11	READER STEP (+ 5 volt)
B12	READER READY
B13	COMMON RAIL
B17	KEYWAY

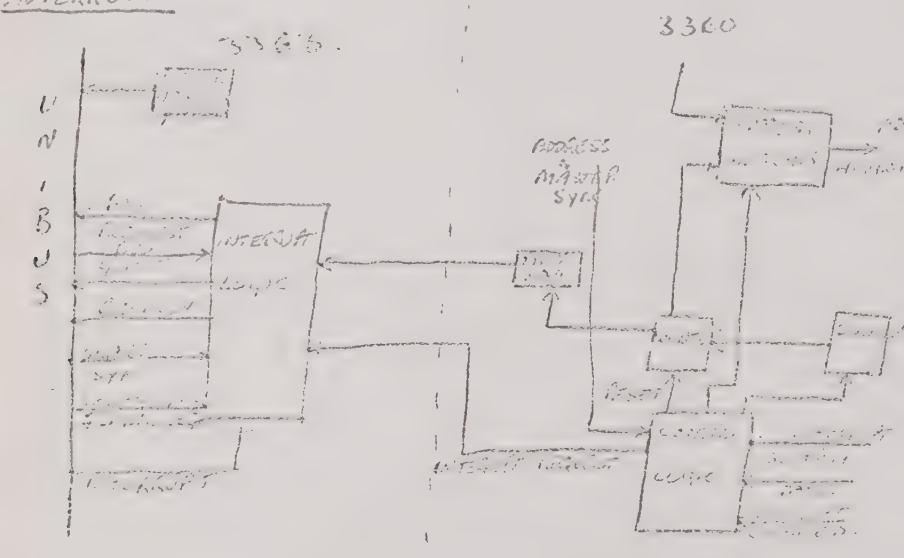
TRANSFER BLOCK DIAGRAM



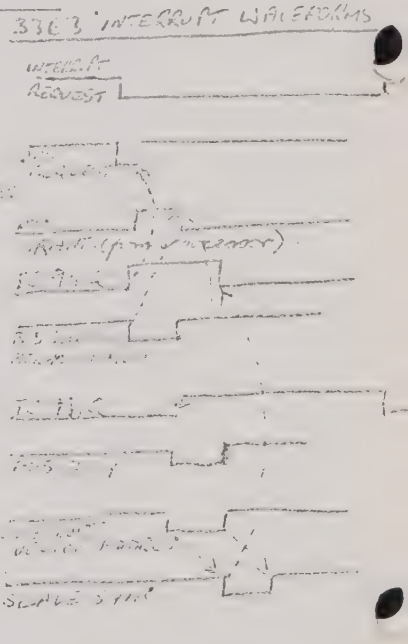
TRANSFER WAVEFORMS



INTERRUPT.

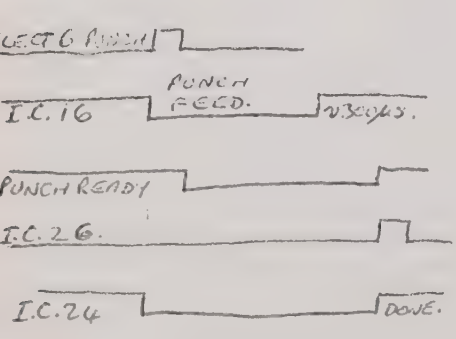


3363 INTERRUPT WAVEFORMS

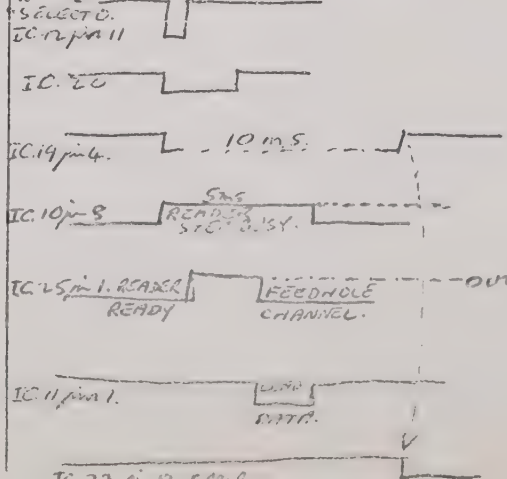


3363 PUNCH & READER INTERFACE

PUNCH



READER.



Series 3 Computer Logger

Theory of Operation

3363 Interface COMPUTER INTERFACE

Address Logic 33639301

Address bits 1 - 10 are routed through buffer stages to the logger.
Address bits 11- 17 are de-coded, with Master Sync, by IC18, to produce an "Address and Master Sync" signal and a "Transfer" signal which go to the 3360 controller.
The C1 line is routed through buffer stages as the logger T2 line.

Information highway buffers 33639301

Data bits 0 - 10 are routed through the Data/Status selector gates and driver stages to the logger Information Highway. Data/Status switching is controlled by address bit 1.(COMPUTER (T1)

Data highway buffers 33639302 SHT. 2.

The logger data highway is fed through Data/Status selector gates, controlled by address bit 1, and then through output gates to the Unibus bits 0 - 11. The output gates are opened when the "Address and Master Sync" signal is present, and the C1 line is high (read) at IC38a.

Data transfer logic 33639301 and 33639302

When the address fed to the logger corresponds with the address decode of one of the logger modules, the module supplies an "Address Valid" signal to the 3360 controller.
After a settling delay the processor generates a "Master Sync" signal, which produces a "Transfer" signal from the 3363 interface to the 3360 controller.
When the 3360 controller has received both the Address Valid and the Transfer signal, it generates a Strobe pulse which fires monostable IC35. 3360 SHT. 1

SHT. 2.

The leading edge of IC35 pulse clocks IC40b which cancels the Transfer signal at IC30a.

The trailing edge of IC35 pulse, through IC38b, clocks IC40a, generating a "Slave Sync" signal to the processor.

Upon receipt of Slave Sync the processor cancels the Master Sync signal, so cancelling the "Address and Master Sync" signal and resetting IC40a and b.

Interrupt control logic 33639302

This contains two flip-flops which step through four stages of operation:

	IC9a	IC9b	State
1	cleared	cleared	Circuit ready
2	set	cleared	Issue Bus Request
3	set	set	Assert Interrupt Line
4	cleared	set	Interrupt finished

Note All logic lines between this circuit and the Unibus, except the Bus Grant line, are low when asserted.

1) Ready condition.

The Interrupt Request line being high when not in use, maintains direct clear inputs to IC9a and IC9b. Bus Grant pulses entering the interface pass via IC8a, IC2c, IC3d, TR1 and IC10a to the Bus Grant output.

If the Interrupt Request line is asserted by the 3360 controller, the request is passed via IC2e and IC3a to the Bus Request output.

2) Bus request state

Upon receipt of a Bus Request, the processor issues a Bus Grant pulse (high) which passes via IC8a and IC2c to clock IC9a on its leading edge. IC9a being set disables the Bus Grant output via IC10b and generates a"Selection Acknowledge" signal to the processor via IC3c.

3) Interrupt State

When the processor receives "Selection Acknowledge" it cancels the "Bus Grant" signal. The Bus Grant signal, through IC8a, IC4b and IC5a clocks IC9b on its trailing edge. IC9a and IC9b both being set cause:

(a) A Bus Busy signal to be produced by IC3b.

(b) The Vector Address and the Interrupt lines to be asserted through IC4a, IC2a and the Vector Address gates.

3) (c) The Selection Acknowledge signal from IC3c to be cancelled.
(d) IC9b clock input to be inhibited by IC4b and IC5a.

4) Interrupt Finished State

The processor receives the Interrupt signal and responds with Slave Sync. The Slave Sync signal passes through IC8c, IC2f, IC5d and IC5c to clear IC9a. This cancels the Bus Busy signal from IC3b and closes the Vector Address and Interrupt gates via IC4a.

The circuit returns to the ready condition when the 3360 Controller removes the Interrupt Request signal.

3360 Computer-Driven Controller CONTROL INTERFACE

Reset Circuit

The Master Reset circuit generates an Initialise signal when power is applied or when an Initialise signal is received from the computer. This signal is fed to the logger highway by IC13c.
The Initialise signal resets the Search flip-flop IC14. It also causes the logger modules to release the Interrupt Search line, which resets IC20a and IC20b through IC16b.

Non-Interrupt Operation

If IC14 is in the reset condition, the Address Gates pass the address input from the 3363 Interface via the Address Drivers to the logger Address Highway.
If an Interrupt Search is in progress, the Address and Master Sync signal releases the set input to IC14, and the leading edge of IC15b pulse resets IC14. This switches the Address Gating circuits to enable the address input from the 3363 interface to pass to the Address Highway.
A logger module which is addressed responds with an Address Valid signal to IC19c which gives a high output during the Transfer signal from the 3363 interface. After a delay produced by R38 and C7, IC21 produces a Strobe pulse which is passed to the logger highway through IC4e and to the 3363 interface via IC4f. The Strobe cancels the Transfer signal, allowing C7 to discharge before another data transfer is requested.

Data and Information Highways

These are connected through the 3360 Controller to the 3363 Interface.

Interrupt Search

This is requested by one or more of the logger modules asserting the Interrupt Search line. If a data transfer is not in progress, the Interrupt Search input sets IC 14 via IC16b and IC18a.
If a data transfer is in progress, IC14 sets when the "Address and Master Sync" signal is removed at the end of the data transfer operation.
When IC14 sets, it triggers IC15a, producing a pulse which passes via IC17a and IC19b to reset IC6 and 7. The trailing edge of IC15a pulse triggers IC15b.

The leading edge of the pulse from IC15b sets IC20b, inhibiting IC17a and enabling IC17c. It also clocks IC20a which will set if IC17b has detected bits 7 and 8 ("Done" and "Interrupt Enabled") set in the Status output of the logger module being addressed. It also clocks IC14 which will reset if the "Address Master Sync" line from the 3363 interface has been asserted, so freezing the Interrupt Search routine.

The trailing edge of IC15b pulse triggers IC15a, unless IC14 has been reset. This repeats the cycle of operations, but pulses from IC15a now pass through IC17c to index the Search Address counter, unless IC20a has been set.

When the interrupting logger module has been detected, IC 20a sets, preventing pulses from passing through IC17a or IC17c. This holds the counter at the address of the interrupting module. The next pulse from IC15b sets IC20b so that, if the logger module ceased to interrupt and the Interrupt Search line remained asserted, the search routine would start again from the beginning.

When IC20a is set, an Interrupt Request is issued to the 3363 interface via IC4d.
The Interrupt Request is removed when the computer has serviced the interrupting logger module, so that it releases the Interrupt Search line.

Address Gating

The Address Gates are controlled by IC14. When an Interrupt Search is in progress, address lines 1 - 8 are fed from the Search Address counter. The T1 and T2 lines are held low (Status, Read) and Address line 9 is high.

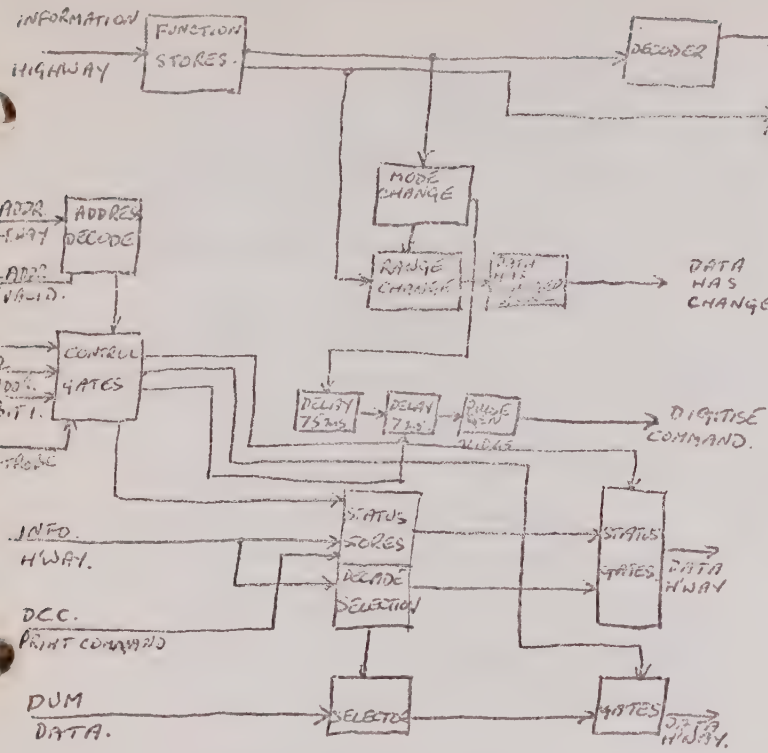
When an Interrupt Search is not in progress, the Address, T1 and T2 lines are fed from the 3363 Interface.

Vector Address

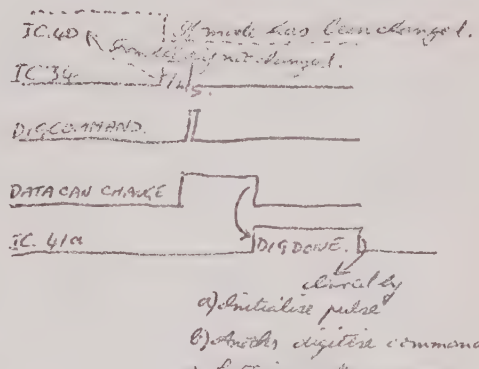
The Vector Address is derived from the Search Address counter IC6 and IC7 by adding 300 (octal) in IC11, and then fed to the 3363 Interface via the drive stages.

3336 DVM INTERFACE.

BOB DUNN

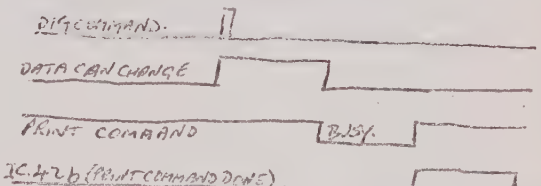


D.V.M. DIGITISATION WAVEFORMS.



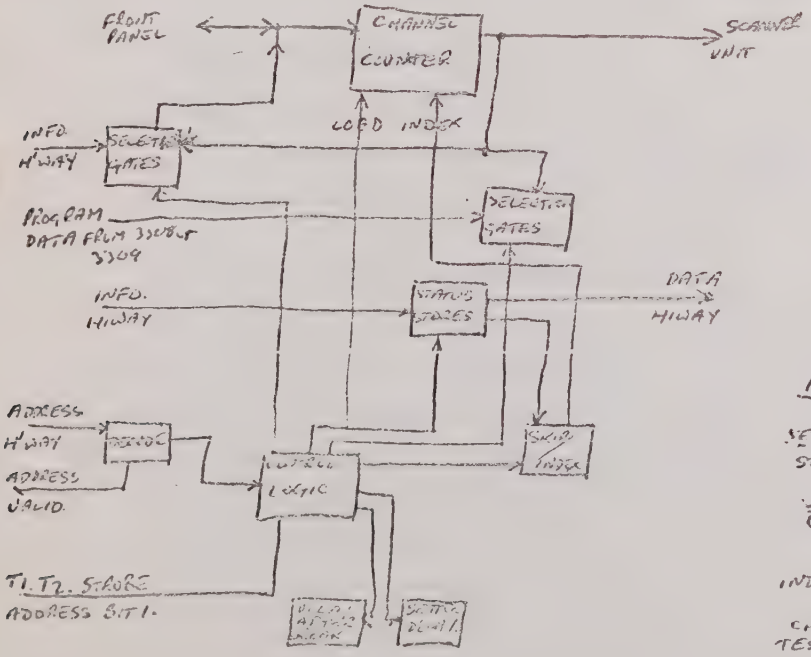
Cleared by.
a) Initialise pulse
b) Another digitise command.
c) Setting mode or range.

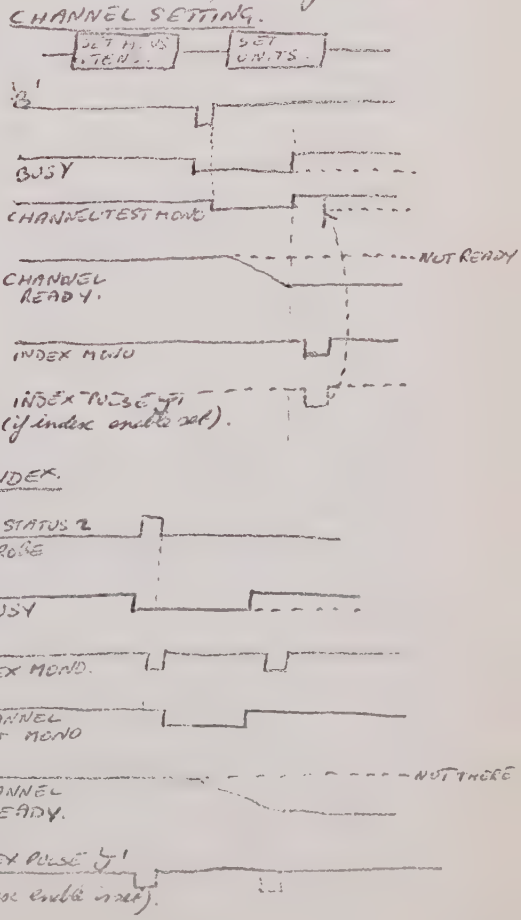
PRINT COMMAND WAVEFORMS.



Cleared by.
a) Initialise pulse.
b) Another dig. cond. pulse.
c) Reading out DVM data.

3353 SCANNER CONTROLLER.





3353 Scanner Controller

Control Signals

A. Select Data In (low)

When the Address Decode IC15 is satisfied, and the T1 line is low (Status), the output of IC26c is high.
If the T1 line is high (Data) when the Address Decode is satisfied, the output of IC26d is high.
When Address bit 1 is high (Receiver), the output of IC25a is high.

Thus, if the T1 line and Address bit 1 are both high, IC25b produces a low output which causes the data selectors IC12, 13 and 14 to select inputs from the Information Highway.

B. Load-Units Pulse (low)

When IC42a is set (Select Units) the output of IC36c is low. If signal A is also low, the output of IC36b is high. The Strobe pulse then passes through IC5e, IC5f and IC37d to provide a low-going pulse which operates the load input of the Units counter IC21, triggers IC39b (Channel Test) and sets IC42b to the "Busy" state via IC41a and IC41c.

C. Clear-Units Pulse (low)

When IC42a is not set and Signal A is low, the output of IC36a is high. This allows the Strobe pulse to pass through IC37b to provide a low-going pulse which drives the clear input of the Units Counter IC21.

D. Load Hundreds and Tens Pulse (low)

The inputs to IC37c are in parallel with the inputs to IC37b, so that IC 37c produces a low-going pulse which operates the load input of the Hundreds and Tens Counters IC19 and IC20.
If IC30b is not set (Program Data Selected), a low input to IC38f releases the output of IC38e, so that a pulse B (Load Units) also produces a pulse D via IC38d.

E. Select Program Data (low)

If IC30b is not set (Program Data Selected) the low input to IC25d gives a high input to IC36d, causing a low output level to be fed to the Highway data selectors IC17 and IC18 selecting program data to be fed to the Data Highway.

F. Enable Units (high)

If the address of the module is recognised by IC15, the T1 line is high and address bit 1 is low, the output of IC25a is low. This is inverted by IC24a and if IC30b is set (Program Data not selected), a low output appears from IC25d. If IC42a is set (Units selected), the output of IC36d is also low, causing IC36a to produce a high output, which enables the output of the Units Counter IC21 to be fed via IC16 to the Data Highway.

G. Enable Highway Data Selectors (low)

If signal F is not present, a high level is fed from IC24f to IC31c. If at the same time the output of IC25a is low, IC31c produces a low output which goes to the enable inputs of the data selectors IC17 and IC18. According to the state of signal E this allows either Hundreds or Tens channel identity outputs or program data to be fed to the Data Highway.

H. Enable Data Selectors (low)

When IC30b is set (Program Data not selected), a low output from IC9d enables the data selectors IC12, IC13 and IC14. The output of IC9d also goes to the Front Panel unit where it inhibits the inputs via PLD.

Note

Signals A to H are generated regardless of the state of the T2 line. Thus in the computer-controlled logger an attempt to read data from the Receiver Data Register causes the Channel Counter to be loaded with a zero input.

Status Store Control Signals

Set Data (low)

When the address is recognised by IC15, the T1 line is high (Data), and the T2 line is high (Set), a Strobe pulse via IC5b produces a low-going pulse at the output of IC32a. This clocks IC42a to complement the Select Units status bit.

COMPUTER

Read Status (high)

When the address is present, the T1 line is low (Status), and the T2 line is low (Read), IC33b is satisfied and IC40e gives a high output which enables the Status Gates to feed the Data Highway.

COMPUTER

Set Status Pulse (high)

When the address is present, the T1 line is low and the T2 line is high (Set), a Strobe pulse passes via IC5c, IC33c and IC40f to generate a high-going pulse which produces the following results:

(a) IC42a is loaded from Information bit 2 via IC11f, IC31b and IC41b.
(b) IC30b is loaded from Information bit 3.
(c) IC35a is loaded from Information bit 1.
(d) IC35b is loaded from Information bit 6.
(e) IC35c is loaded from Information bit 8 via IC11a.
(f) IC35d is loaded from Information bit 5 via IC11c.

Set Status 2 Pulse (high)

When the Set Status pulse occurs, if address bit 1 is low, a high-going pulse is produced by IC26a. This triggers IC39a (Index) and sets IC42b to the "Busy" state via IC11b, IC41a and IC41c.

The Skip/Index Loop

This comprises two monostables, IC39a which generates Index pulses, and IC39b which produces a Channel Test delay period.
It may be started in two ways:

(a) By a Load Units pulse B, which triggers IC39b and sets IC42b to the "Busy" state. The end of the pulse from IC39b triggers IC39a via a delay circuit R33, C10.

The leading edge of IC39b pulse clocks IC30a (Transceiver Busy), setting it, if the Transceiver Busy input is low.

If IC30a is not set, the trailing edge of IC39b pulse clocks IC42b via IC25c. IC42b is cleared, if one of the following conditions on the input to IC32b.

(i) IC35b (Disable Skip) is set.

(ii) The Front Panel last channel input is low.

(iii) The Channel Ready input is low.

If IC42b is not cleared, the pulse from IC39A passes through IC26b to trigger IC39B. It is also passed through IC33a, unless IC30b is set (Transceiver Busy), producing an Index Counter pulse J which increments the Channel Counter.

(b) A set status 2 pulse triggers IC39a and sets IC42b to the "Busy" condition. Unless IC 30a (Transceiver Busy) is set, or IC35a (Index Enable) is not set, the pulse from IC39a passes through IC26b and IC33a to produce an Index Counter pulse J. The trailing edge of IC35a pulse triggers IC35b and the circuit then runs as before.

Transceiver Sync Pulse (low)

This is derived via IC37a and IC40c from either the Load Units pulse B or the Index Counter pulse J.

Delay After Break

If IC35d (Call Relays) is set, the Load Units pulse B or the Index Counter pulse J triggers IC34a via IC37a and IC29b. The output of IC31d is high when IC35d (Call Relays) is not set, or when IC34a pulse is present. If IC42b (Busy) is set, the output of IC31d is clamped low by IC38c.

When IC31d output is high, the relays are de-energised by calling the 800 and 400 drive lines simultaneously via IC9e and IC9f.
When IC31d output is low, IC24d feeds a "Busy" signal to the Status Gate IC23d, and IC40d supplies an "Energise Transceiver" signal (high).

Settle Delay

IC34b is triggered when IC35d (Call Relays) is set and IC42b (Busy) is cleared.

Busy Output (Status)

Bit 1 is fed to the Status Gate IC22c when IC42b (Busy) is set, or during the Delay after Break pulse from IC34a via IC29c and IC29d.

Done Output (Status)

Bit 7 is fed to the Status Gate IC23b when the Busy output is not present, unless the Settle Delay pulse from IC34b is present.

Interrupt Search

The Interrupt Search line is called when IC35c (Interrupt Enable) is set and the Done output is present.

Channel Ready Signal

The Channel Ready signal from the scanner unit is fed via IC38b to the Status Gate IC22a (bit 4).

Initialise

An Initialise pulse has the following effect:

(a) It clears IC30a (Transceiver Busy)
(b) It clears IC30b (Select Program Data)
(c) It clears IC42a (Select Units)
(d) It clears IC42b (Busy)
(e) It sets IC35a (Index Enable)
(f) It sets IC35b (Disable Skip)
(g) It clears IC35c (Interrupt Enable)
(h) It clears IC35d (Call Relays).

See Block Diagrams & Wave Forms on page 3.6.

3336 Master Voltmeter Interface

Control Gates

Control Decoder IC 27 is fed with four signals.

(a) T2 line (Read)

(b) T1 line (Status)

(c) Address bit 1 (Source)

(d) The output of Address Decoder IC21.

IC27 generates the following control states:

(a) Read Source Status (decode 0)

This signal, via IC16d, enables the output gates for the Print Command Status Stores.

(b) Set Source Status (decode 1)

This signal allows a Strobe pulse to pass through IC28d, to load IC14 (Decade Selection Store) via IC43f and IC31d, and to load IC42a (Print Command Interrupt Enable) from the Information Highway.

(c) Read Source Data (decode 2)

In the Series 3 Computer Logger, pins D2 and D3 are linked, and this signal, via IC7, allows the selected decades to be fed to the Data Highway.

It also enables the Strobe pulse to pass via IC28c, IC35d and IC20b to clear IC42b (Print Command Done).

N.B. This signal is not used in Compact 33 systems.

(d) Set Source Data (decode 3)

In the Compact 33 system, pins D1 and D2 are linked. This signal enables IC14 (Decade Selection Store) to pass data from the Information Highway and, via IC7, enables the selected decades to be fed to the Data Highway.

It also enables the Strobe pulse to pass via IC28c, IC35d and IC20b to clear IC42b (Print Command Done).

N.B. This signal is not used in the computer-based logger.

(e) Read Receiver Status (decode 4)

This signal, via IC32b, enables the output gates for the Digitise Status Stores.

(f) Set Receiver Status (decode 5)

This signal allows the Strobe pulse to pass through IC28b. The pulse from IC28b, via IC43d, loads IC41b (Digitisation Interrupt Enable) from the Information Highway.

If Information Highway bit 1 (Digitise Command) is present, the pulse from IC28b passes via IC33c to carry out the following functions:

(i) Set IC38 (Digitisation Busy), so triggering the Digitise Command circuit.

(ii) Clear IC41a (Digitisation Done) via IC35a, IC35b and IC36b.

(iii) Clear IC42b (Print Command Done) via IC35a, IC35b and IC20b.

(g) Set Receiver Data (decode 7)

This signal allows the Strobe pulse to pass through IC28a, IC33a and IC10d to load the Function Stores from the Information Highway.

It also allows the Strobe pulse to pass through IC35c, to clear IC41a (Digitisation Done), via IC35b and IC36b.

If the state of one of the Mode Function Stores IC22a, IC24a or IC24b is changed, this change is detected by IC37c, IC37d or IC37b respectively, which pass a high level to IC44b, IC33b or IC44c, allowing the Set Receiver Data pulse, via IC18a, to trigger IC40.

If the state of one of the Function Stores has changed, a low level will appear on the D input of IC29a, and the Set Receiver Data pulse will produce a Data Has Changed output via IC18d.

Mode Commands

The Mode command information is stored in IC22a, IC24a and IC24b and decoded by IC17 to drive the Mode command inputs of the Fan-out unit.

Range Commands

Range command information is stored in IC23a, IC23b and IC29b, and fed to the Fan-out unit via IC18e, IC18c and IC18b.

Changes of range are detected by IC36a, IC36c and IC36d. They are combined with changes of mode by means of IC31c, IC43a, IC43b, IC43c, IC44a and IC44d. The output of these gates is loaded into IC29a (Data Has Changed) by the Set Receiver Data pulse.

Digitise Command Circuit

A Digitise Command sequence is started by a Set Receiver Status pulse, which sets IC38 (Digitisation Busy), if Information Highway bit 1 is present.

This triggers IC34 (7 milliseconds) unless IC40 is in operation. At the end of IC34 delay period, IC32 (pulse generator) produces a 50-microsecond Digitise Command pulse, which is fed to the Fan-out unit.

If a change of mode takes place, IC40 is triggered (75 milliseconds). If IC38 is now set, IC34 triggers at the end of the pulse from IC40.

Data Can Change Circuit

During the ramp-up period of the digital voltmeter, the Data Can Change signal goes high. It is fed through IC39b and sets IC41a (Digitisation done) on its trailing edge.

When IC41a sets, it clears IC38 (Digitisation Busy).

Print Command Circuit

During the ramp-down period of the digital voltmeter, the Print Command line goes low. It is fed via IC39a to IC25b as a Busy Status signal. The trailing edge of the signal, via IC43e, sets IC42b (Print Command Done)

Interrupt Search Line

This line can be asserted by two means.

(a) When IC41a (Digitisation Done) and IC41b (Digitisation Interrupt Enable) are both set.

(b) When IC42a (Print Command Interrupt Enable) and IC42b (Print Command Done) are both set.

Initialise

An Initialise pulse has the following actions.

(a) Clears IC41a (Digitisation Done) via IC9c, IC16c and IC36b.

(b) Clears IC42b (Print Command Done) via IC9c, IC16c and IC20b.

(c) Clears IC38 (Digitisation Busy), IC41b (Digitisation Interrupt Enable) and IC42a (Print Command Interrupt Enable) via IC9c.

(d) Clears the Function Stores IC22, IC23, IC24 and IC29.

Decade Selection

The 3336 Interface presents data from the Digital Voltmeter to the Data Highway in BCD code, in four two-decade bytes. The eight input gates IC1, 2, 3, 4, 5, 6, 11 and 12 each handle one bit of the four bytes.

Selection of the Bytes is controlled by IC14 which is loaded from bits 2 and 3 of the information highway. The state of IC14 is decoded by IC8, and the outputs of IC8 are encoded by the S links and fed via IC13 to the Status output gates IC31a and IC31b.

IC7 is enabled by the Read Source Data signal, which allows the output of IC8 to enable one Byte to be fed to the Data Highway through the Decade Selector Gates and highway driver stages.

3363 TEST PROCEDURE

Equipment required: -

PDP-11 computer — 3359 logger rack with
3360 and 3331 power supply
3387 cable

Plug the 3363 into the computer and connect it by means of a 3387 cable to the 3360 in the 3359 rack.

1) Initialise

Examine PLA pin A 14 of the 3360 with a 'scope. Check that pressing HALT/START on the computer changes the level from + 5 V to 0 V.

2) Addressing tests

Run the following program: -

Address		Contents		
000004		000006	.+ 2	
000006		000002	RTI	
any	012706	START:	MOV # 600, R 6	
	000600			
	013700		MOV @ # SWR, R 0	
	177570			
	005710		TST @ R0	
	000772		BR START	

Set bit 15 in the switch register, and then check that each bit of the switch register changes the level on the 3360 during the address period.

Switch Register	3360 PLA
Bit 10	Pin A 9
9	A 8
8	A 7
7	A 6
6	A 5
5	A 4
4	A 3
3	A 2
2	A 1
1	A 10 (inverted level)

3) Status output transfer

Fit 3353 scanner controller (address 0)

Run the program as follows: -

Address		Data	
000300		000302	.+2
000302		000002	RTI
any(1000)	012706	START:	MOV #600, SP (Stack Pointer)
	000600		
	013737		MOV @#SWR, @#164000
	177570		
A	164000		
	000774		BR START

Check that the waveforms on the 3360 PLA are switched by the following switch register bits: -

3360 PLA	Switch Register
Pin B 9	Bit 0
B 10	1
B 11	2
B 12	8
B 13	9
B 14	10
B 15	7
B 16	6

4) Data output transfer

Change the contents of location A in the above program from 164000 to 164002. Repeat test 3.

The following table now applies: -

3360 PLA	Switch Register
Pin B 9	Bit 0
B 10	1
B 11	2
B 12	3
B 13	4
B 14	5
B 15	6
B 16	7

Measure the pulse width at IC 35 (1-2.5 µs) Pin 6 on 3363 in Computer

5) Data input transfer

Load and read channel identity in the 3353 scanner controller as follows: -

(a) Load address 164000
(b) Deposit 000000
(c) Load address 164002
(d) Deposit 000377
(e) Examine
(f) Deposit 000377
(g) Load address 164006
(h) Examine should be 000377
(i) Deposit
(j) Examine should be 000360

Repeat, depositing 000000 at steps (d) and (f).

The result should be 000000 at steps (h) and (j).

6) Status input transfer

Load and examine bits 1, 2, 6, 9 and 10 of register 164000. EXCEPT BIT 7

Check that each can be loaded with 0 and 1, and that all other bits are 0.

7) Interrupt test

Run a system interrupt test program, addressing the scanner controller and DVM on interrupt.

3360 TEST PROCEDURE

Equipment required: -

Series 3 logger with PDP-11

3363 and connecting cable
3359 and power supply + cable
3336 and DVM + cable
3353

1) Address output tests

Connect the 3360, in the 3359 frame, to the 3363 in the PDP-11. Insert no other modules in the frame.

(a) Halt the computer. Connect Interrupt search (PLA) pin A 16 of the 3360 to common rail with a short link. Measure the pulse widths produced on IC 15.

IC 15 pin 5 250 - 400 nS
IC 15 pin 13 650 - 1000 nS.

(b) Examine the waveforms on the address lines.

PLA pins A 1 - A 8 switching
A 9 - high
A 10 low
A 11 low
A 12 high

PLB pins A 11-A 17 switching. Decrease in frequency

(c) Remove the shorting link and run the following program: -

Address		Contents	
000004		000006	
000006		000002	
any	012706	Start:	MOV #600, R 6
	000600		
	013700		MOV @ #SWR, R0
	177570		
	005710		TST @ R0
	000774		BR [redacted]

Set switch register to 164000. Check that the waveforms on the address lines are modified by the switch register as follows: -

PLA pin A 1	PDP-11 bit 2
A 2	3
A 3	4
A 4	5
A 5	6
A 6	7
A 7	8
A 8	9
A 9	10
A 10	1 (inverted)
A 11	low during address period
A 12	high " " "

(d) Repeat test (c) with the shorting link between pin A 16 and common rail. Search oscillations should appear on PLA pins A 1 to A 8, between the address periods.

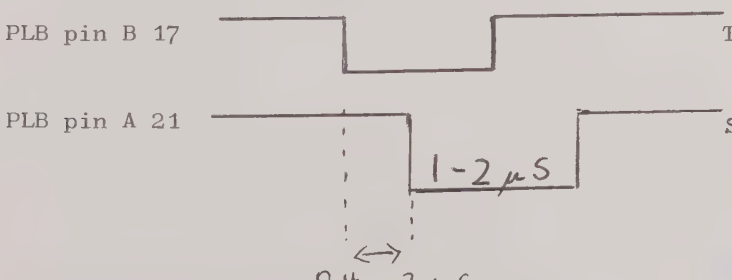
2) Data transfer tests

Insert the 3336 (Address 164010) in the logger frame and run the following program: -

```
013737      MOV @#SWR, @#164012
177570
164012
000774      BR.-6
```

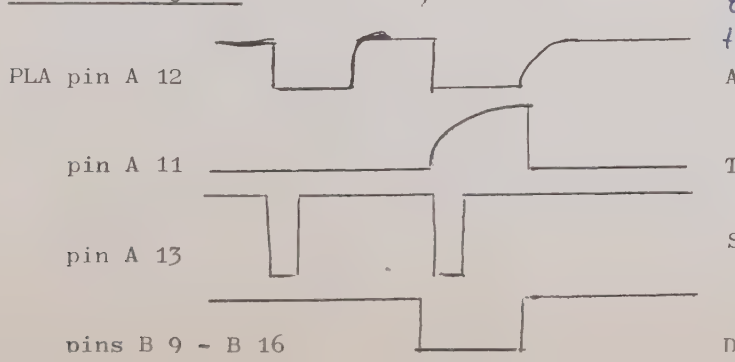
Examine the following signals: -

(a) Strobe delay and pulse widths.



(b) Transfer Signals

Pulse should have risen to 3V by the arrival of the strobe pulse leading edge



Set on switch register 0- to scope

The data pulses on pins B 9 to B 16 are controlled by switch register bits 0 to 7 respectively.

3) Master reset

Monitor the +5V supply and PLA pin A 14.

(a) Check that the master reset line goes to OV when HALT/START are pressed on the computer. If not wish to start keep HALT down.

(b) Switch off the logger power for 30 seconds. Check that, on switching on, the master reset line remains at 0 V for a short time after the + 5 V supply has appeared. Not relicable e not important as above (a)

4) Data test

Fit the 3353 scanner controller (address 164000). Load and read the data bits in the channel identity register as follows: -

(a) Load address 164000
(b) Deposit 000000
(c) Load address 164002
(d) Deposit 000377
(e) Examine
(f) Deposit 000377
(g) Load address 164006
(h) Examine should be 000377
(i) Deposit to compliment status BIT 1
(j) Examine should be 000360

Repeat, depositing 000000 at steps (d) and (f).
The result should be 000000 at steps (h) and (j).

5) System test

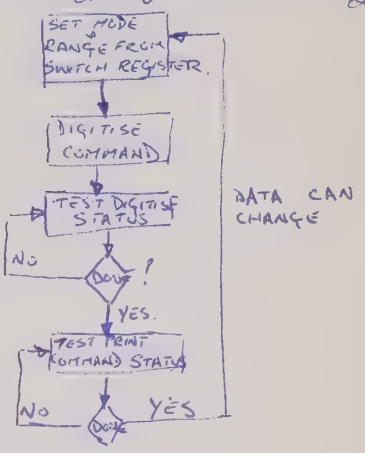
Run system test programs with and without interrupt.

SIMPLE TEST PROGRAMS

Digital Voltmeter Imterface only

```
1000    013737      MOV @ # SWR, @ # 164012
2       177570
4       164012
6       005237      INC @ # 164010
10      164010
12      105737      TSTB @ # 164010
14      164010
16      100375      BPL .-4
20      105737      TSTB @ # 164014
22      164014
24      100375      BPL. -4
26      000764      BR 1000
```

Set DVM range from SW Reg.



Set DVM range from SW Reg (interrupt).

```
1200    012706      MOV # 600, R6
2       000600
4       013737      MOV @ # SWR, @ # 164012
6       177570
10      164012
2       012737      MOV # 101, @ # 164010
4       000101
6       164010
20      000001      WAIT
2       012737      MOV # 100, @ # 164014
4       000100
6       164014
30      000001      WAIT
2       000762      BR 1200


1040    005037      CLR @ # 164000
2       164010
4       000002      RTI


1070    005037      CLR @ # 164014
2       164014
4       000002      RTI


310     001040
        000200
        001070
        000200
```

Digital Voltmeter and Scanner.

Set channel from SWR 15 - 4 Press start to set new channel.

h. t. u.
100, 10, 1.

```
1400    005037      CLR @ # 164000
   2    164000
   4    013700      MOV @ # SWR, RØ
   6    177570
  10    000300      SWAB RØ
   2    010037      MOV RØ, @ # 164002
   4    164002
   6    013737      MOV @ # SWR, 164002
  20    177570
   2    164002
   4    012701      MOV # 40, R1
   6    000040
  30    005301      DEC R1
   2    001376      BNE. -2
   4    105737      TSTB @ # 164000
   6    164000      BP
  40    100015      BELL
   2    012737      MOV # 1000, @ # 164000
   4    001000
   6    164000
  50    105737      TSTB @ # 164000
   2    164000
   4    100375      BPL. -4
   6    005237      INC @ # 164010
  60    164010
   2    133737      BIT B @ # 164010, @ # 164014
   4    164010
   6    164014
  70    100374      BPL. -6
   2    000742      BR 1400
   4    105737 BELL: TSTB @ # TPS
   6    177564
 500    100375      BPL. -4
   2    012737      MOV # 7, TPB
   4    000007
   6    177566
 510    000733
```

Scan all channels, DVM range set from SW Reg.

```
2000    013737      MOV @ # SWR, @ # 164012
   2    177570
   4    164012
   6    005237      INC @ # 164010
  10    164010
   2    105737
   4    164010
   6    100375      BPL. -4
  20    012737      MOV # 1001, @ # 164004
   2    001001
   4    164004
   6    105737      TSTB @ # 164014
  30    164014
   2    100375      BPL. -4
   4    000761      BR 2000
```

Scan all channels Interrupt

```
2200    012706      MOV # 600, SP
   2    000600
   4    013737      MOV @ # SWR, @ # 164012
   6    177570
  10    164012
   2    012737      MOV # 101, @ # 164010
   4    000101
   6    164010
  20    000001      WAIT
   2    012737      MOV # 1101, @ # 164004
   4    001101
   6    164004
  30    000001      WAIT
   2    012737
   4    000101
   6    164014
  40    000001      WAIT
   2    000760      BR 2200

2260    042737      BIC # 100, @ # 164000
   2    000100
   6    164000
   4    000002      RT1

300     2260
         200
        2260
         200
```

3324 CABLE

3369 INTERFACE TO FACIT HIGH SPEED PUNCH

3369		FACIT PUNCH
SK 1		PLA
B 1	Bit 4	5
B 2	" 3	4
B 3	" 7	8
B 4	" 6	7
B 5	" 0	1
B 6	" 2	3
B 7	" 5	6
B 8	" 1	2
B 9	COMMON RAIL	25
B 10	TAPE FEED	11
B 11	PUNCH READY	12
	LINK	(9
		(24

3323 CABLE

3369 INTERFACE TO TREND HIGH SPEED READER

3369		TREND READER
SK2		
B 1	Bit 7	24
B 2	" 4	19
B 3	" 5	6
B 4	" 2	7
B 5	" 6	22
B 6	" 0	20
B 7	" 1	9
B 8	" 3	8
B 11	STEP	14
B 12	READY	18
B 13	COMMON RAIL	(13 (16 (21

3328 CABLE

3331 RACK-MOUNTED POWER SUPPLY TO 3359 CHASSIS

3331		3359
SKA		PLA
A	OP 5	A
B	OP 4	B
C	- 16 v	C
D	COMMON RAIL	D
E	9 v	E
F	CLOCK	F
G	5 v	G
H	5 v (SENSE)	H
J	COMMON RAIL (SENSE)	J

3378 CABLE

3336 TO DVM A210/211/212/213

3336 SKB		A214 PLA
A 1	COMMON RAIL	HH
A 2	800,000 Not Used	b
A 3	400,000 Not Used	a
A 4	200,000 Not Used	Z
A 5	100,000	Y
A 6	POLARITY POSITIVE	d
A 7	80,000	X
A 8	40,000	W
A 9	20,000	V
A 10	10,000	U
A 11	8,000	T
A 12	4,000	S
A 13	2,000	R
A 14	1,000	P
A 15	800	N
A 16	400	M
A 17	200	L
A 18	KEYWAY	-
A 19	80	J
A 20	40	H
A 21	20	F
A 22	10	E
B 1	PRINT COMMAND LEVEL	v
B 2	DATA CAN CHANGE	x
B 3	PULSE SAMPLE	t
B 4	100	K
B 5	COMMAND AUTO RANGE	y
B 6	COMMAND REMOTE	r
B 7	RATE 25/Sec) BINARY	EE
B 8	RATE 100/Sec)	FF
B 9	MODE AC) BINARY	AA
B 10	MODE OHMS)	BB Goes to mapping in Comfast for a Low.
B 11	DATA IS CHANGED	w
B 12	COMMAND RANGE 4)	p
B 13	COMMAND RANGE 2) BINARY	n
B 14	COMMAND RANGE 1)	m
B 15	RANGE OUTPUT 1	f
B 16	RANGE OUTPUT 2	h
B 17	RANGE OUTPUT 4	j
B 18	KEYWAY	~
B 19	1	A
B 20	2	B
B 21	4	C
B 22	8	D

3387 CABLE

3360 TO 3363

3360		3363	
SKB		SKE	SKF
A 1	ADDRESS 01	B 1	
A 2	" 02	B 2	
A 3	" 03	B 3	
A 4	" 04	B 4	
A 5	" 05	B 5	
A 6	" 06	B 6	
A 7	" 07	B 7	
A 8	" 08	B 8	
A 9	" 09	B 9	
A 10	" 10	B 10	
A 11	VECTOR 02	B 17	
A 12	" 03	B 16	
A 13	" 04	B 15	
A 14	" 05	B 14	
A 15	" 06	B 13	
A 16	" 07	B 12	
A 17	" 08	B 11	
A 20	[redacted] T2	B 22	
A 21	STROBE		B 18
A 22	O V	A1-A22	
B 1	DATA 1		B 9
B 2	" 2		B 10
B 3	" 3		B 11
B 4	" 4		B 13
B 5	" 5		B 14
B 6	" 6		B 15
B 7	" 7		B 16
B 8	" 8		B 17
B 9	INFO 1		B 1
B 10	" 2		B 2
B 11	" 3		B 3
B 12	" 4		B 4
B 13	" 5		B 5
B 14	" 6		B 6
B 15	" 7		B 7
B 16	" 8		B 8
B 17	TRANSFER	B 21	
B 18	ADDR. & MASTER SYNC.	B 20	
B 19	INTER REQ	B 19	
B 20	INITIALISE		B 20
B 22	O V		A1-A22

3390/3393 CABLE

3353 TO 33 SERIES SCANNER

3353		3304
SKB		SKA
12 A	100	18 A
11 A	200	19 A
14 A	400	20 A
13 A	800	17 A
16 A	10	9 B
15 A	20	10 B
18 A	40	8 B
17 A	80	16 A
20 A	1	20 B
19 A	2	19 B
22 A	4	18 B
21 A	8	17 B
20 B	SKIP	2 B
1 A	C/R - 1	1 B
9 A	1	15 A
8 A	2	14 A
3 A	4	3 A
2 A	8	12 A
5 A	10	11 A
4 A	20	10 A
7 A	40	9 A
6 A	80	8 A

3333		
1	9 volts	1A to 5A
2	0 volts	3B to 7B

DVM		SKD
High	Analogue Bus 2	12 A
Low	" " 1	13 A
Guard	" " G	14 A
	" " 3	11 A

3304

N.B. [redacted] (Earth to C/R 2) in free-standing Scanner Units.

SKT A 7B to 16B of cable

3398 CABLE

3336 TO DVM's A200/203/220/223

3336		A204
SKB		PLA
A 1	COMMON RAIL	HH
A 2	80,000 Not used	X
A 3	40,000 Not used	W
A 4	20,000 Not used	V
A 5	10,000	U
A 6	POLARITY POSITIVE	d
A 7	8,000	T
A 8	4,000	S
A 9	2,000	R
A 10	1,000	P
A 11	800	N
A 12	400	M
A 13	200	L
A 14	100	K
A 15	80	J
A 16	40	H
A 17	20	F
A 18	KEYWAY	-
A 19	8	D
A 20	4	C
A 21	2	B
A 22	1	A
B 1	PRINT COMMAND LEVEL	v
B 2	DATA CAN CHANGE	x
B 3	PULSE SAMPLE	t
B 4	10	E
B 5	COMMAND AUTO RANGE	y
B 6	COMMAND REMOTE	r
B 7	RATE 25/Sec) BINARY	EE
B 8	RATE 100/Sec)	FF
B 9	MODE AC) BINARY	AA
B 10	MODE OHMS)	BB
B 11	DATA IS CHANGED	w
B 12	COMMAND Range 4)	p
B 13	COMMAND Range 2) BINARY	n
B 14	COMMAND Range 1)	m
B 15	RANGE OUTPUT 1	f
B 16	RANGE OUTPUT 2	h
B 17	RANGE OUTPUT 4	j
B 18	KEYWAY	-
B 19	NOT USED) C/R in Fanout	b
B 20	NOT USED) L.S.D. in	a
B 21	NOT USED) 3336	Z
B 22	NOT USED)	Y

IC No.	TYPE	PIN No Vcc	PIN No C/R	IC No.	TYPE	PIN No Vcc	PIN No C/R
1, 3, 6, 10, 20 31, 32, 36	DEC 8881	14	7	13, 16, 21, 25	SN7406	14	7
2, 7, 19, 24, 37	SN7404	14	7	18	SN7430	14	7
4, 30, 38	SN7400	14	7	23, 28, 29, 39	SN7401	14	7
5, 33, 34	SN7402	14	7	35	SN74121N	14	7
8, 11, 12, 14, 15 17, 22, 26, 27	DEC 380A	8	1				
9, 40	SN7474	14	7				

ADDRESS LOGIC

ADDRESS DECODE

ADDRESS BUFFER

CONTROL SIGNAL GATE

DATA INPUT BUFFERS

DATA OUT STATUS/DATA SWITCHING

INFORMATION HIGHWAY OUTPUT BUFFERS

STATUS

DATA

SWITCH in CONTROL INTERFACE

SWITCH OFF INTERUPTS.

SCHLUMBERGER		USED ON	JOB STAGE	DEVELOPMENT ✓ PRODUCTION	
© THE SCHLUMBERGER ELECTRONIC DOCUMENTATION			TITLE	PDP11 INTERFACE	
ISS	DATE	CHANGE	SCALE	DIMNS	
01			DR'N M E C	DATE 2-1-73	DRAWING NUMBER D33639301
			CH'D	DATE	
			APP'D	DATE	

D33639301

ENABLE ON DATA

FROM 3360

DATA HIGHWAY

PROGRAMMED TRANSFER CONTROL LOGIC

DATA IN STATUS/DATA SWITCHING

OUTPUT GATES

TO PROCESSOR

DEVICE INTERRUPT VECTOR ADDRESS

VECTOR ADDRESS GATES

BUS INTERRUPT CONTROL

CHECK SOLDERED THROUGH BOARD

BUS GRANT 'B' LINKS

LINKS 'A' & 'B' SHOWN CONNECTED FOR PRIORITY LEVEL 4

BUS GRANT JL

BUS 00 05 07

INTRPT LOW

SELECTION ACKNOWLEDGE.

SIMILAR PAGE 6-30 PERIPHERALS.

Schlumberger	USED ON	JOB STAGE	DEVELOPMENT ✓ PRODUCTION
ISS 01 DATE CHANGE		TITLE	PDP 11 INTERFACE
	SCALE DIMNS.		
	DRN MAC DATE 9.12.72	DRAWING NUMBER	D 33639302
	CH'D DATE		
	APP'D DATE		

D33639302

IC No	TYPE	PIN No Vcc	PIN No C/R	IC No	TYPE	PIN No Vcc	PIN No C/R	IC No	TYPE	PIN No Vcc	PIN No C/R
1,2,3,4,13	7406	14	7	14,20	7474	14	7	18	7400	14	7
5,8,9,10,12	7401	14	7	15	74123	16	8	19	7402	14	7
6,7	7493	5	10	16, 22, 23	7404	14	7	21	7412	4	7
11	7483	5	12	17	7410	14	7				

T2

ADDRESS INPUT

SET/READ C1

+9V

+5V

0V

INITIALISE

ADDRESS & MASTER SYNC

INTERRUPT SEARCH

TRANSFER

ADDRESS VALID

DATA HIGHWAY (FROM LOGGER)

INFORMATION HIGHWAY (FROM COMPUTER)

MASTER RESET

INTERRUPT SEARCH OSCILLATOR

SEARCH FLIP FLOP

INPUT INVERTER

START SEARCH

INDEX GATE

RESET GATE

SEARCH ADDRESS COUNTER

STROBE MONOSTABLE

INTERRUPT FOUND

ADDRESS VALID

DONE

INTERRUPT ENABLED

ADDRESS GATES

ADDRESS DRIVERS

VECTOR ADDRESS DRIVERS

OUTPUT INVERTER

OUTPUT INVERTERS

MASTER RESET

ADDRESS

DATA STROBE

STATUS

LOW READ

STROBE

T3 EXECUTE STROBE

TO LOGGER.

DATA HIGHWAY (TO COMPUTER)

INFORMATION HIGHWAY (TO LOGGER)

TO LOGGER

TO COMPUTER

SOLARTRON Schlumberger

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ISS	DATE	CHANGE
01		

SCALE

DRN M E C

DATE 2-12-77

CHK D

APP'D

TITLE COMPUTER-DRIVEN CONTROL UNIT

DRAWING NUMBER 03360930 01

DEVELOPMENT / PRODUCTION

NO 03360

L ON STATUS
H = DATA → PROCESSOR
L = DATA → PROCESSOR
L = READ H = SET

ADDRESS DECODE

ALL MADE IN COMPUTER LOGGER

COMMAND GATES — DE MAN'S

H. STATUS

H. DATA

L. DATA IN FROM PROCESSOR

L. DATA OUT

L SET DATA STROBE

READ STATUS

L SET STATUS

DATA FROM PROCESSOR

TO CHANNEL COUNTER AND SELECTION GATES IC 12,13,14 PIN 1 DRG 2

TO CHANNEL COUNTER AND SELECTION GATES IC 21 PIN 1 DRG 2

L LOAD UNITS.

L LOAD 100s, 10

TO CHANNEL COUNTER AND SELECTION GATES IC 21 PIN 13 DRG 7

TO CHANNEL COUNTER AND SELECTION GATES IC 19, 20 PIN 1 DRG 2

H 100, 10 SEL C.T.

H UNITS O/P SEL.

TO DATA HIGHWAY GATES IC 17, 18 PIN 1 DRG 2

L ENABLES 100s + 10s PROG DATA

TO DATA HIGHWAY GATES IC 17, 18 PIN 15 DRG 2

L INHIBIT PROG DATA FROM F.P.A

TO CHANNEL COUNTER AND SELECTION GATES IC 12, 13, 14, PIN 15 DRG 2

SET STATUS TO STROBE WHEN ADDRESS BIT 1 SET

STATUS STORES

INDEX ENABLE

HIGH AT ENABLE

H AT CALL

CALL RELAYS.

BIT 1 ON COMPUTER

H AT S

SEL. UNITS.

CLOCKS ON TRAILING EDGE

CLEAR INITIALISE

L AT S

SEL. PROG. DATA

H SET STATUS!

BIT 2 ON COMPUTER

TRANSCEIVER BUSY L AT B

L AT B BUSY

L AT D DISABLE SKIP

H AT E INTERRUPT ENABLE

CLR.

SKIP/INDEX LOOP

L INDEX CLOCK COUNTER

TO CHANNEL COUNTER AND SELECTION GATES IC 21 PIN 8 DRG 2

INDEX 115-2 mS

12-1 mS

'DELAY AFTER BREAK' MONOSTABLE

130 - 160 mS

RELAYS ENERGISE

'SETTLE' MONOSTABLE

10 - 15 mS

L INTERRUPT ENABLE

STATUS GATES

DONE

L CALL(E)

400 CHANNEL DRIVE

800 CHANNEL DRIVE

ENERGISE (TRANSCEIVER)

DONE

DATA A

DATA B

ACCEPT/SKIP CHANNEL

RELAYS CALLED

SKIP ENABLED

CHANNEL CHANGE BUSY

INTERRUPT ENABLED

INTERRUPT SEARCH

ADDRESS VALID

INHIBIT F/P CHANNEL

TRANSCEIVER SYNC PULSE

SLOGGER & COMPUTER

SLOGGER & COMPUTER

Schlumberger

ISS | DATE | CHANGE
01

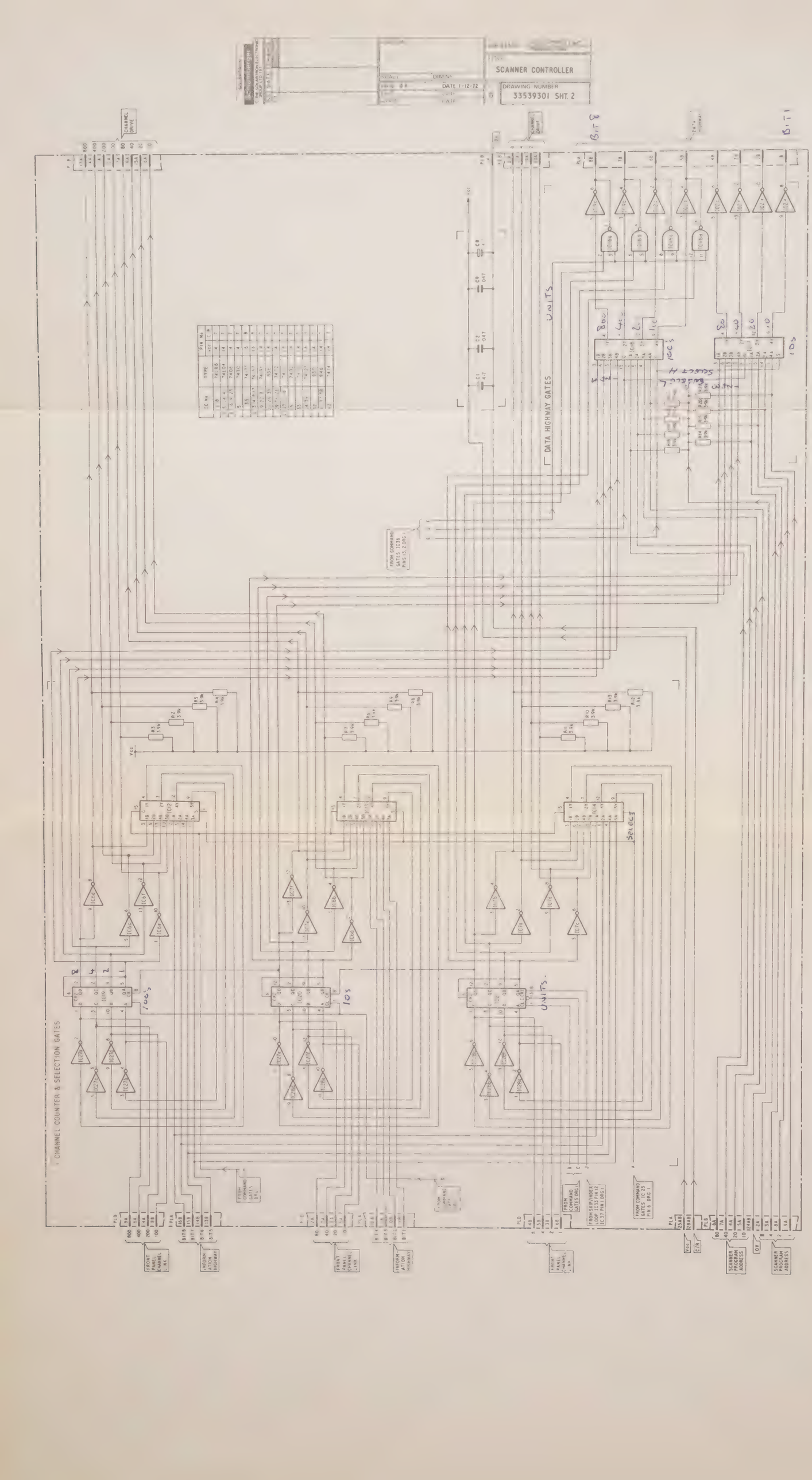
SCALE | DRWN M A S | DATE 4-12-72 | CHKD | APP'D | DATE

TITLE: SCANNER CONTROLLER

JOB STAGE — DEVELOPMENT / PRODUCTION

DRAWING NUMBER 3353950I SHT. 1

D


SCANNER CONTROLLER
DRAWING NUMBER
33539301 SHT. 2
DATE 1-12-72
DATA HIGHWAY GATES
UNITS
CHANNEL COUNTER & SELECTION GATES
Select
FROM COMMAND GATES (IC5) PINS 12 (IC6)
FROM COMMAND GATES (IC5) PINS 9 (IC6)
FROM COMMAND GATES (IC5) PINS 1 (IC6)
FROM SCANNER (IC5) PIN 12
FROM SCANNER (IC5) PIN 9
FROM SCANNER (IC5) PIN 1
FRONT COMMAND GATES (IC6)
FRONT PANEL CHANNEL LINK
INTERFACE HIGHWAY
SCANNER PROGRAM ADDRESS
CHANNEL WRITE
DATA HIGHWAY

INFO HIGHWAY

FUNCTION STORES

TO STATUS STORES DRG 2 IC 41 42 PINS 12 2

NOT USED

CHANGE OF DATA DETECTOR

ENCODER

CALL AUTO RANGE
CALL REMOTE
CALL 25 R/S
CALL 100 R/S
CALL A C VOLTS
CALL OHMS

CHANGE OF DATA STORE

MODE OR RANGE HAS CHANGED
CALL RANGE 4
CALL RANGE 2
CALL RANGE 1

IC14 PIN 7 SHT 2. PIN 6

INITIALIZE IC9 PIN 6

FROM CONTROL GATES DRG 2 IC 10 PIN 8

ADDRESS DECODER

IC No	TYPE	PIN No Vcc	PIN No C/R
7	7402	14	7
8	7400	14	7
9	7407	14	7
10	7407	14	7
11	7454	14	7
12	7454	14	7
13	7420	14	7
14	7475	5	12
15	7404	14	7
16	7404	14	7
17	7442	16	8
18	836	14	7
19	7486	14	7
20	7486	14	7
21	7430	14	7
22	7474	14	7
23	7474	14	7
24	7474	14	7
25	7401	14	7

1-6 7454

IC No	TYPE	PIN No Vcc	PIN No C/R
26	7401	14	7
27	7442	16	8
28	7402	14	7
29	7474	14	7
31	7401	14	7
32	836	14	7
33	846	14	7
34	74121	14	7
35	7402	14	7
36	7486	14	7
37	7486	14	7
38	7472	14	7
39	7413	14	7
40	74121	14	7
41	7474	14	7
42	7474	14	7
43	836	14	7
44	846	14	7

DIGITISE COMMAND AND DELAY

FROM STATUS STORES DRG 2 IC 25 38 PINS 2 8

47kpf FOR 100 CHANNELS A SEC.

PERIOD. 1 to 10 μ S.

period 7mS

Period 75mS

DIGITISE COMMAND

TO CONTROL GATES DRG 2 IC 27 PIN 12

ADDRESS VALID

Schlumberger	USED ON	JOB STAGE	DEVELOPMENT ✓ PRODUCTION
SOLARTRON	CHANGE	TITLE	D.V.M. INTERFACE
	SCALE	DIMNS	
	DRN A C	DATE 6 11 72	DRAWING NUMBER D33369301 SHT 1 OF 2
	CH D	DATE	
	APP D	DATE	

D33369301 SHT 1 OF 2

D2 to 3 Computer Logger
D1 to 2 Compact 33

53,6,7,8 MADE IN COMPUTER LOGGER
READ OUT SAME BIT PATTERN AS PUT IN

COMPUTER BIT 0

ENABLE DIGITISE

DATA CAN CHANGE

L=READ
H=SET

L=STATUS
H=DATA

TRANSFER 2

TRANSFER 1

ADDRESS

L. DATA TO REGISTER
H. " FROM "

FROM ADDRESS DECODER IC 015 PIN 8

STROBE 1

INITIALISE

PRINT COMMAND

POLARITY

RANGE

ENABLE/ DIGITISE GATES

CONTROL GATES

TP3

SHT 1

TO FUNCTION SELECTOR DRG 1

FROM FUNCTION SELECTOR BIT 8 DRG 1

DIGITISE DONE

DIG. BUSY

DIG INTRUPT ENABLE

PRINT COMMAND DONE

PRINT COMMAND INTRUPT ENABLE

STATUS STORES

TO DIGITISE COMMAND B DELAY IC 34 PIN 5 DRG 1

DIGITISE/DATA BUSY

DIGITISE/DATA DONE

INTERRUPT ENABLE DIGITISE/DATA

INTERRUPT ENABLE

DECADE SELECTOR

FROM FUNCTION SELECTOR IC 15 PIN 12 DRG 1

FROM FUNCTION SELECTOR IC 15 PIN 10 DRG 1

DATA 1 READY

DATA 2 READY

DECADE GATING

C/R

BIT 8
BIT 7
BIT 6
BIT 5
BIT 4
BIT 3
BIT 2
BIT 1

Schlumberger		USED ON	JOB STAGE: DEVELOPMENT ✓ / PRODUCTION
	ISS 01 DATE CHANGE	SCALE DIM'NS	TITLE: DVM INTERFACE
		DR'N A C DATE 7 12 72	DRAWING NUMBER: 03369301 SHT 2 OF 2
		CH'D DATE	
		APP'D DATE	

03369301 SHT 2 OF 2

INPUT INVERTERS

OUTPUT LATCHES

INFORMATION HIGHWAY

BIT 1
BIT 2
BIT 3
BIT 4
BIT 5
BIT 6
BIT 7
BIT 8

MASTER RESET INVERTERS

MASTER RESET

EXT INTERRUPT

STROBE L

TRANSFER 1

ADDRESS BIT 11

TRANSFER 2

STATUS GATES

SET STATUS

STATUS STORE

SEL BIT 1

SEL BIT 2

SPARE

INTERROGATE

CONTROL DECODER

INTERRUPT GATES

DECADE 4

DATA RX

DATA TR

LK8

LK9

LKC

To Unit Wait

ADDRESS HIGHWAY

VALID ADDRESS DETECTOR

ADDRESS LINKS

READ STATUS

READ STATUS GATES

I.C. No.	TYPE	PIN No	
		Vcc	C/R (0v)
1 8	7486	14	7
2 36	7430	14	7
3 48 49 55 56	* BT1B	14	7
4–7 11–14 18–21 25–28	7545	8	4 (C/R2B)
9 22 24 31 47 54	7404	14	7
10 29 43	7420	14	7
15 38 50	7400	14	7
16	7474	14	7
17	74122	14	7
23 44–46 51–53	7401	14	7
30 32–35 39–42	7475	5	12
37	7442	16	8

* +24V CONNECTED TO PIN 13

+24V
+5V
0V

INPUT DATA GATES

EXTERNAL DATA INPUT

DATA HIGHWAY GATES

REGISTER 0
REGISTER 1
REGISTER 2
REGISTER 3

INTERRUPT SEARCH
SPECIAL INTERRUPT
ADDRESS VALID
DATA HIGHWAY

SOLARTRON Schlumberger

USED ON

JOB STAGE: DEVELOPMENT / PRODUCTION

TITLE: DIGITAL I/P O/P INTERFACE

SCALE | DIMNS

DRN A C DATE 14.12.72

CH'D DATE

APP'D DATE

DRAWING NUMBER D33649301

D33649301

READER INTERRUPT ENABLE

READER STEP GENERATOR

PUNCH INTERRUPT CONTROL

PUNCH FEED GENERATOR

READER INTERFACE

PUNCH DRIVE

Paper Reader Status

Paper Punch Buffer

From the Reader

IC No	TYPE	PIN No C/R	PIN No Vcc	IC No	TYPE	PIN No C/R	PIN No Vcc	IC No	TYPE	PIN No C/R	PIN No Vcc
1,2,17,22	8881	7	14	10,15,24	7474	7	14	19	74123	8	16
3,4,	7475	12	5	11,16,20,26	7421	7	4	25	8836	7	4
7,8,18	3804	1	8	13	7404	7	14	5			
9,12,21,23	7400	7	14	14	7402	7	14				

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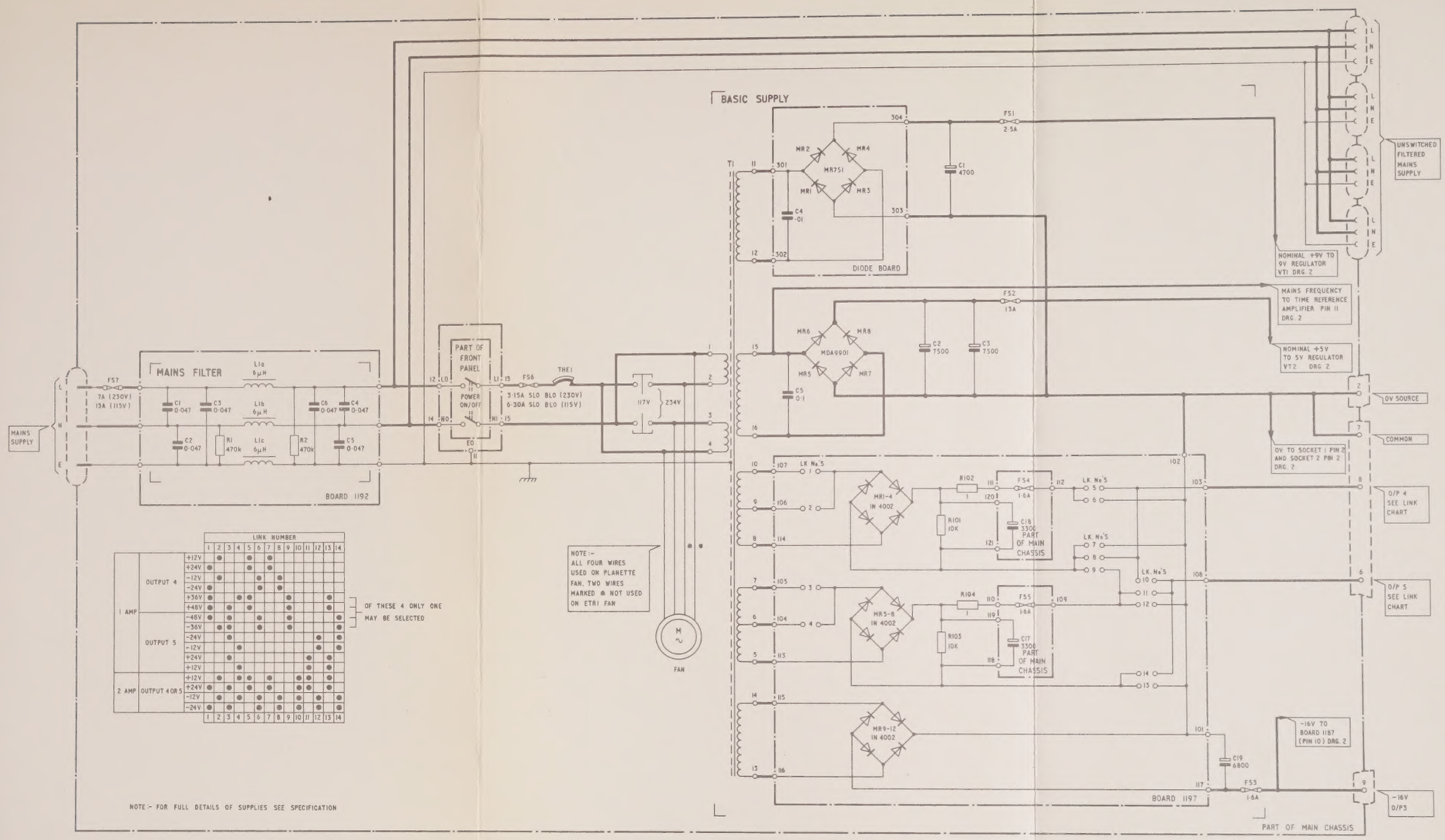
ISS	DATE	CHANGE
01		

APP'D | CH'D | DR'N | SCALE | USED ON
DATE | DATE | M.E.C. | DIMNS | P0P11
DATE 12-12-72

JOB STAGE — DEVELOPMENT / PRODUCTION

TITLE: HIGH SPEED PUNCH/ READER INTERFACE

DRAWING NUMBER
D33699301

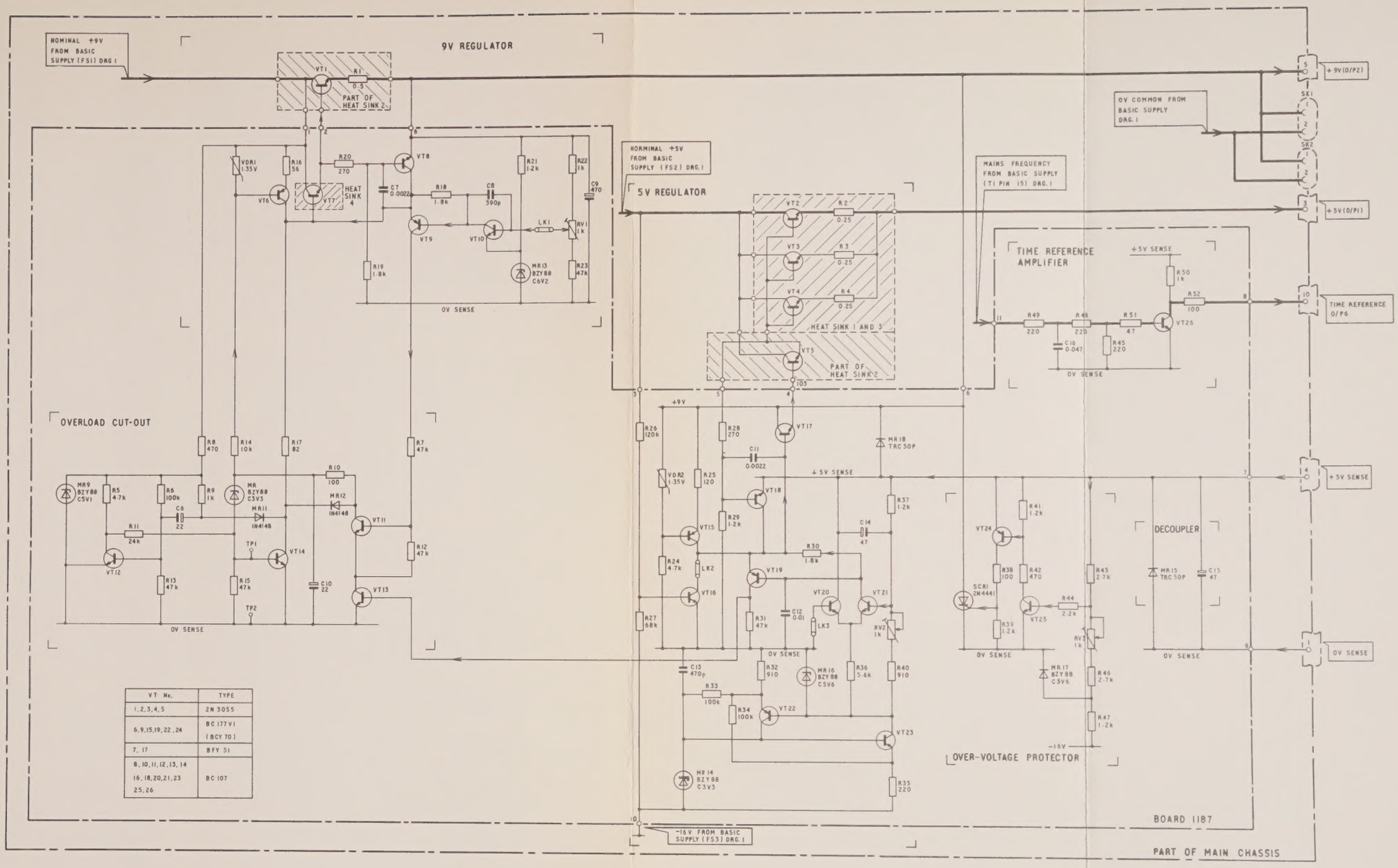


NOTE :- FOR FULL DETAILS OF SUPPLIES SEE SPECIFICATION

SCHLUMBERGER © THE SCHLUMBERGER ELECTRONICS GROUP LTD 1972	ISS	DATE	CHANGE	USED ON
	01			

JOB STAGE	DEVELOPMENT ✓ / PRODUCTION
TITLE	POWER UNIT
SCALE	DIM'NS
DR'N G.V.N.	DATE 7-12-72
CH'D	DATE
APP'D	DATE
DRAWING NUMBER	3333700I

3333700I



VT No.	TYPE
1, 2, 3, 4, 5	2N 3055
6, 9, 15, 19, 22, 24	BC 177 VI (BCY 70)
7, 17	BFY 51
8, 10, 11, 12, 13, 14 16, 18, 20, 21, 23 25, 26	BC 107

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ISS	DATE	CHANGE
01		

USED ON

SCALE DIM'NS

DR'N J.P. DATE 1-12-72

CH'D DATE

APP'D DATE

JOB STAGE DEVELOPMENT ✓ PRODUCTION

TITLE POWER UNIT

D 33337002

33337002

MP MASTER
MA24227